Z86C72

CMOS Z8 MCU with 16 KB ROM/748-Byte RAM

Product Specification

PS002402-0408

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
April 2008	02	Changed 44-pin QFP to 44-pin LQFP. Updated Zilog logo and Disclaimer section Changed Ordering Information, Figure 2 title, and Figure 37 Deleted Document Information Page	All page 85, page 3, and page 84
February 2002	01	Original Issue	All

Table of Contents

Architectural Overview

Equipped with 748 bytes of general-purpose RAM, the Z86C72 is a ROM-based solution incorporating Zilog's popular Z8® MCU technology. The use of external memory enables these Z8 microcontrollers to be used where code flexibility is required. Zilog's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-ups. The Z86C72 product line offers easy hardware/software system expansion with cost-effective and low power consumption.

The features of Z86C72 include:

- Low Power Consumption—80 mW (typical)
- Two Standby Modes:
  - STOP
  - HALT
- 31 Input/Output Lines
- Automatic External ROM Access Beyond 16K
- Special Architecture to Automate Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse RECEPTION
- Five Priority Interrupts
  - Three External
  - Two Assigned to Counter/Timers
- Low-Voltage Detection and Standby Mode
- Programmable Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC (mask option), or External Clock Drive
- Mask Selectable Pull-Up Transistors (100 KΩ) on Ports 0, 2, 3
  - Port 2 Pull-Ups are Bit Selectable
  - Pull-Ups are Automatically Disabled as Outputs
- 32-kHz Oscillator Mask Option

Functional Block Diagram

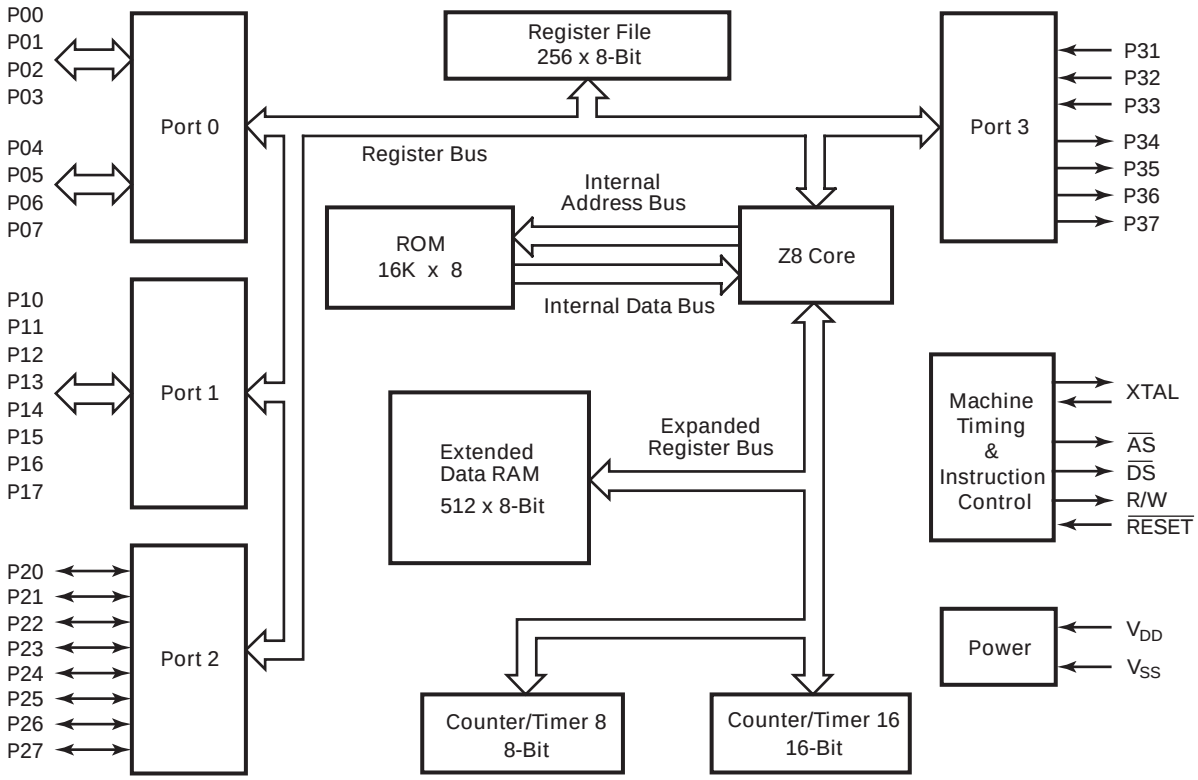


Figure 1. Functional Block Diagram

Pin Description

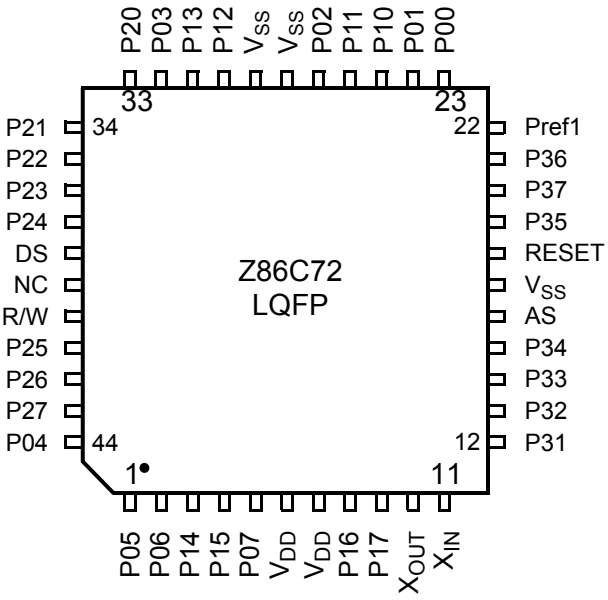


Figure 2. 44-Pin LQFP Pin Assignments

Table 1. Pin Identification by Pin Number

Pin No	Symbol	Direction	Description
1	P05	Input/Output	
2	P06	Input/Output	
3	P14	Input/Output	
4	P15	Input/Output	
5	P07	Input/Output	
7	V_{DD}		Power Supply
7	V_{DD}		Power Supply
8	P16	Input/Output	
9	P17	Input/Output	
10	X_{OUT}	Output	Crystal, Oscillator Clock
11	X_{IN}	Input	Crystal, Oscillator Clock
12	P31	Input	IRQ2/Demodulator Input
13	P32	Input	IRQ0
14	P33	Input	IRQ1
15	P34	Output	T8 output
16	AS	Output	Address Strobe
17	V_{SS}		Ground
18	RESET	Input	Reset
19	P35	Output	T16 output
20	P37	Output	
21	P36	Output	T8/T16 output
22	Pref1	Input	Comparator 1 Reference
23	P00	Input/Output	Port 0 is Nibble Programmable
24	P01	Input/Output	Port 0 can be configured as A15–A8 external program ROM/DATA Address Bus
25	P10	Input/Output	Port 1 is byte programmable
26	P11	Input/Output	Port 1 can be configured as multiplexed A7–A0/D7–D0 external program ROM/ Data Address/Data Bus

Pin No	Symbol	Direction	Description
27	P02	Input/Output	Port 0 can be configured as a mouse/ trackball input
28	V_{SS}		Ground
29	V_{SS}		Ground
30	P12	Input/Output	
31	P13	Input/Output	
32	P03	Input/Output	
33	P20	Input/Output	Port 2 pins are individually configurable as input or output
34	P21	Input/Output	P20 can be configured as demodulator input
35	P22	Input/Output	
36	P23	Input/Output	
37	P24	Input/Output	
38	DS	Output	Data Strobe
39	NC		Not Connected
40	R/$\overline{W}$	Output	READ/WRITE
41	P25	Input/Output	
42	P26	Input/Output	
43	P27	Input/Output	
44	P04	Input/Output	

Table 2. Pin Identification by Pin Number

Pin No	Symbol	Direction	Description
16	AS	Output	Address Strobe
38	DS	Output	Data Strobe
39	NC		Not Connected
23	P00	Input/Output	Port 0 is Nibble Programmable
24	P01	Input/Output	Port 0 can be configured as A15–A8 external program ROM/DATA Address Bus
27	P02	Input/Output	Port 0 can be configured as a mouse/ trackball input
32	P03	Input/Output	
44	P04	Input/Output	
1	P05	Input/Output	
2	P06	Input/Output	
5	P07	Input/Output	
25	P10	Input/Output	Port 1 is byte programmable
26	P11	Input/Output	Port 1 can be configured as multiplexed A7–A0/D7–D0 external program ROM/ Data Address/Data Bus
30	P12	Input/Output	
31	P13	Input/Output	
3	P14	Input/Output	
4	P15	Input/Output	
8	P16	Input/Output	
9	P17	Input/Output	
33	P20	Input/Output	Port 2 pins are individually configurable as input or output
34	P21	Input/Output	P20 can be configured as demodulator input
35	P22	Input/Output	
36	P23	Input/Output	
37	P24	Input/Output	
41	P25	Input/Output	

Pin No	Symbol	Direction	Description
42	P26	Input/Output	
43	P27	Input/Output	
12	P31	Input	IRQ2/Demodulator Input
13	P32	Input	IRQ0
14	P33	Input	IRQ1
15	P34	Output	T8 output
19	P35	Output	T16 output
21	P36	Output	T8/T16 output
20	P37	Output	
22	Pref1	Input	Comparator 1 Reference
40	R/$\overline{W}$	Output	READ/WRITE
18	RESET	Input	Reset
7	V_{DD}		Power Supply
7	V_{DD}		Power Supply
17	V_{SS}		Ground
28	V_{SS}		Ground
29	V_{SS}		Ground
11	X_{IN}	Input	Crystal, Oscillator Clock
10	X_{OUT}	Output	Crystal, Oscillator Clock

Operational Description

The Z86C72 is specifically designed for high-security operation—the ROM/ROMless pin is disabled and not accessible externally. The device operates in ROM mode only, which prevents the device from going into ROMless mode (grounding the former ROM/ ROMless pad results in a malfunction of the Z8). Additionally, the contents of the user RAM are cleared upon entering the factory test mode, thus making any previously-stored data unreadable.

The Z86C72 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and high-security applications.

For applications demanding powerful I/O capabilities, the Z86C72 provides 31 pins of dedicated input and output. These lines are grouped into four ports. Each port consists of eight lines (Port 3 features seven lines) and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are five basic address spaces available to support a wide range of configurations: Program Memory, Register File, Expanded Register File, Extended Data RAM and External Memory. The register file and Extended Data RAM are composed of 768 bytes of total RAM. It includes four I/O port registers, 16 control and status registers and 748 General-Purpose registers. The Expanded Register File consists of two additional register banks (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86C72 family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers. See Figure 3. Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Note: *All Signals with an overline are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.*

Counter/Timer Block Diagram

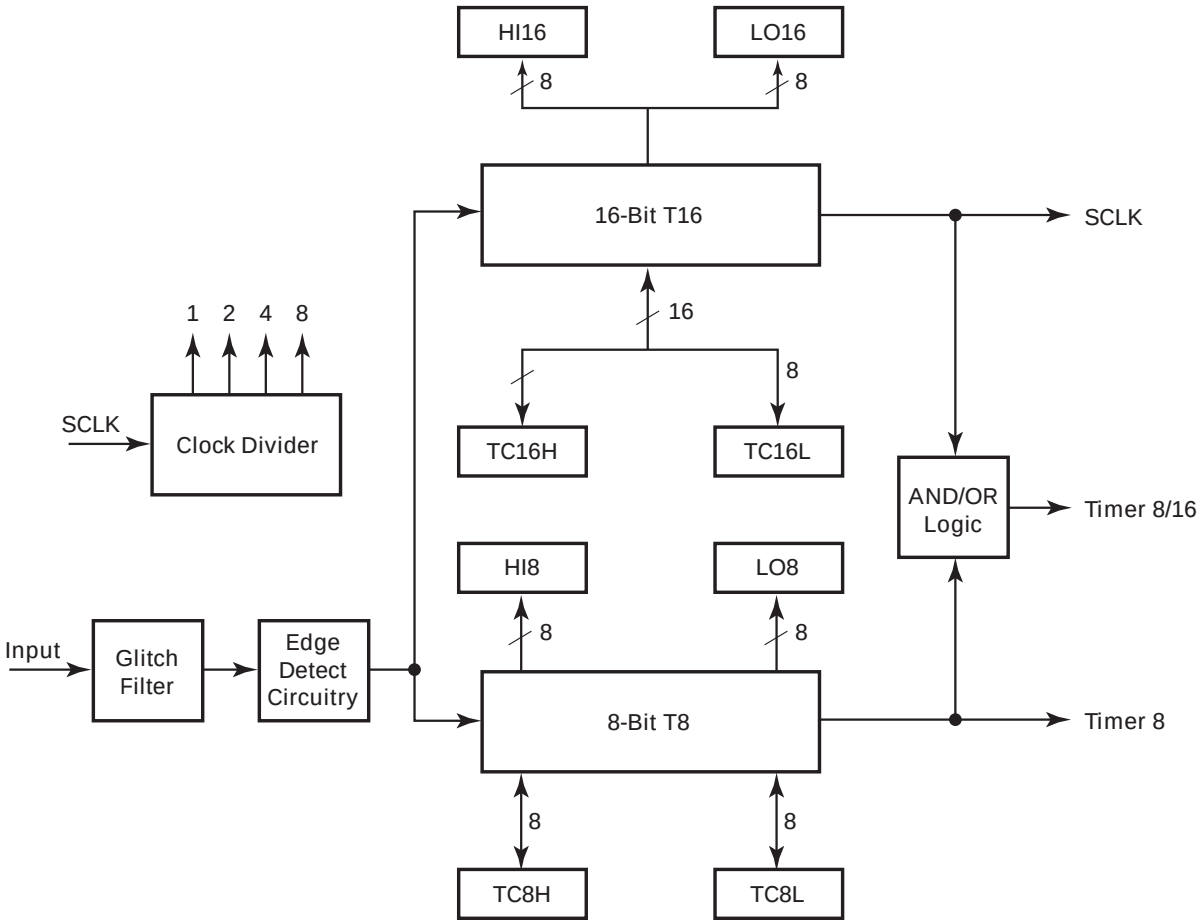


Figure 3. Counter/Timer Block Diagram

Counter/Timer Register Description

Table 3. Counter/Timer Register Description

Expanded Register Group D			
(D)H0C	Reserved	(D)H05	TC8H
(D)H0B	HI8	(D)H04	TC8L

Table 3. Counter/Timer Register Description (Continued)

Expanded Register Group D			
(D)H0A	LO8	(D)H03	Reserved
(D)H09	HI16	(D)H02	CTR2
(D)H08	LO16	(D)H01	CTR1
(D)H07	TC16H	(D)H00	CTR0
(D)H06	TC16L		

HI8(D)H0B. This register holds the captured data from the output of the 8-bit Counter/Timer0. This location is typically used to hold the number of counts when the input signal is 1.

Bit Field	Bit Position	R/W	Description
T8_Capture_HI	76543210	R	Captured Data
		W	No Effect

LO8(D)H0A. This register holds the captured data from the output of the 8-bit Counter/Timer0. This location is typically used to hold the number of counts when the input signal is 0.

Bit Field	Bit Position	R/W	Description
T16_Capture_LO	76543210	R	Captured Data
		W	No Effect

HI16(D)H09. This register holds the captured data from the output of the 16-bit Counter/Timer16. This location holds the MS-Byte of the data.

Bit Field	Bit Position	R/W	Description
T16_Capture_HI	76543210	R	Captured Data
		W	No Effect

LO16(D)H08. This register holds the captured data from the output of the 16-bit Counter/Timer16. This location holds the LS-Byte of the data.

Bit Field	Bit Position	R/W	Description
T16_Capture_LO	76543210	R	Captured Data
		W	No Effect

TC16H(D)H07. Counter/Timer2 MS-Byte Hold Register.

Bit Field	Bit Position	R/W	Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)H06. Counter/Timer2 LS-Byte Hold Register.

Bit Field	Bit Position	R/W	Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)H05. Counter/Timer8 High-Hold Register.

Bit Field	Bit Position	R/W	Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)H04. Counter/Timer8 Low Hold Register.

Bit Field	Bit Position	R/W	Description
T8_Level_LO	76543210	R/W	Data

Table 4. CTR0 (D)00h Counter/Timer8 Control Register

Bit Field	Bit Position	R/W	Value	Description
T8_Enable	7	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	6	R/W	0	Modulo-N
			1	Single Pass

Table 4. CTR0 (D)00h Counter/Timer8 Control Register (Continued)

Bit Field	Bit Position	R/W	Value	Description
Time_Out	5	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T8_Clock	4,3	R/W	00	SCLK
			01	SCLK ÷ 2
			10	SCLK ÷ 4
			11	SCLK ÷ 8
Capture_INT_Mask	2	R/W	0	Disabled Data Capture Interrupt
			1	Enable Data Capture Interrupt
Counter_INT_Mask	1	R/W	0	Disabled Data Capture Interrupt
			1	Enable Data Capture Interrupt
P34_Out	0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note: *Indicates the value upon Power-On Reset.

CTR0: Counter/Timer8 Control Register Description

T8 Enable. This field enables T8 when set to 1.

Single/Modulo-N. When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Time-Out. This bit sets when T8 times out (a terminal count is reached). To reset this bit, a 1 must be written to this location. *This method is the only way to reset the status condition; therefore, care must be taken to reset this bit prior to enabling the counter/timers.*

Note: *Care must be taken when utilizing the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (DEMODULATION mode). These instructions use a READ–MODIFY–WRITE sequence, in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value, and eventually written back into the registers.*

Example: When the status of bit 5 is 1, a reset condition occurs.

T8 Clock. This bit defines the frequency of the input signal to T8.

Capture_INT_Mask. Setting this bit allows interrupts when data is captured into either LO8 or HI8 upon a positive or negative edge detection in DEMODULATION mode.

Counter_INT_Mask. Setting this bit allows interrupts when T8 exhibits a time out.

P34_Out. This bit defines whether P34 is used as a normal output pin or the T8 output.

CTR1(D)H01. This bit controls the functions in common with the T8 and T16.

Table 5. CTR1(D)H01 Counter/Timer T8/T16

Field	Bit Position		Value	Description
Mode	7	R/W	0*	Transmit Mode
			1	Demodulation Mode
P36_Out/Demodulator_Input	6	R/W		Transmit Mode
			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/Edge _Detect	5,4	R/W	Transmit Mode	
			00	AND
			01	OR
			10	NOR
			11	NAND
			Demodulation Mode	
			00	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

Table 5. CTR1(D)H01 Counter/Timer T8/T16 (Continued)

Field	Bit Position		Value	Description
Transmit_Submode/Glitch_Filter	3,2	R/W	Transmit Mode	
			00	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
			Demodulation Mode	
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	16 SCLK Cycle
Initial_T8_Out/Rising_Edge	1	R/W	Transmit Mode	
			0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
			Demodulation Mode	
			0	No Rising Edge
			1	Rising Edge Detected
			0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/Falling _Edge	0	R/W	Transmit Mode	
		R	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
			Demodulation Mode	
		W	0	No Falling Edge
			1	Falling Edge Detected
			0	No Effect
			1	Reset Flag to 0

Note: *Indicates the value upon Power-On Reset

CTR1 Register Description

Mode. If this field is 0, the Counter/Timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

P36_Out/Demodulator_Input. In TRANSMIT mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

T8/T16_Logic/Edge _Detect. In TRANSMIT mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND). In DEMODULATION mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter. In TRANSMIT mode, this field defines whether T8 and T16 are in PING-PONG mode or in independent NORMAL OPERATION mode. Setting this field to NORMAL OPERATION mode terminates the PING-PONG mode operation. When set to 10, T16 is immediately forced to 0. When set to 11, T16 is immediately forced to 1.

In DEMODULATION mode, this field defines the width of the glitch that should be filtered out.

Initial_T8_Out/Rising_Edge. In TRANSMIT mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This condition ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION mode, this bit is set to 1 when a rising edge is detected in the input signal. To reset the bit, a 1 must be written to this location.

Initial_T16 Out/Falling _Edge. In Transmit mode, if 0, the output of T16 is set to 0 when it starts to count. If 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in NORMAL or PING-PONG mode (CTR1, D3–D2). When this bit is set, T16_OUT is set to the opposite state of this bit. This setting ensures that when the clock is enabled, a transition to the initial state is set by CTR1, D0.

In DEMODULATION mode, this bit is set to 1 when a falling edge is detected in the input signal. To reset the bit, a 1 must be written to this location.

Note: *Modifying CTR1, D1–D0 while the counters are enabled causes unpredictable output from T8/T16_OUT.*

Table 6. CTR2 (D)H02 Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	6	R/W	Transmit Mode	
			0	Modulo-N
			1	Single Pass
			Demodulation Mode	
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	5	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	4,3	R/W	00	SCLK
			01	SCLK ÷ 2
			10	SCLK ÷ 4
			11	SCLK ÷ 8
Capture_INT_Mask	2	R/W	0	Disable Data Capture Interrupt
				Enable Data Capture Interrupt
Counter_INT_Mask	1	R/W	0	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P35_Out	0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Note: *Indicates the value upon Power-On Reset.

CTR2 Description

T16_Enable. This field enables T16 when set to 1.

Single/Modulo-N. In TRANSMIT mode, when set to 0, the counter reloads the initial value when terminal count is reached. When set to 1, the counter stops when the terminal

count is reached. In DEMODULATION mode, when set to 0, T16 captures and reloads on detection of all the edges; when set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see T16 Demodulation Mode.

Time_Out. This bit sets when T16 times out (terminal count reached). To reset the time-out, a 1 must be written to this location.

T16_Clock. This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask. Setting this bit allows interrupts when data is captured into LO16 and HI16.

Counter_INT_Mask. Set this bit to allow interrupt when T16 times out.

P35_Out. This bit defines whether P35 is used as a normal output pin or T16 output.

Counter/Timer Functional Blocks

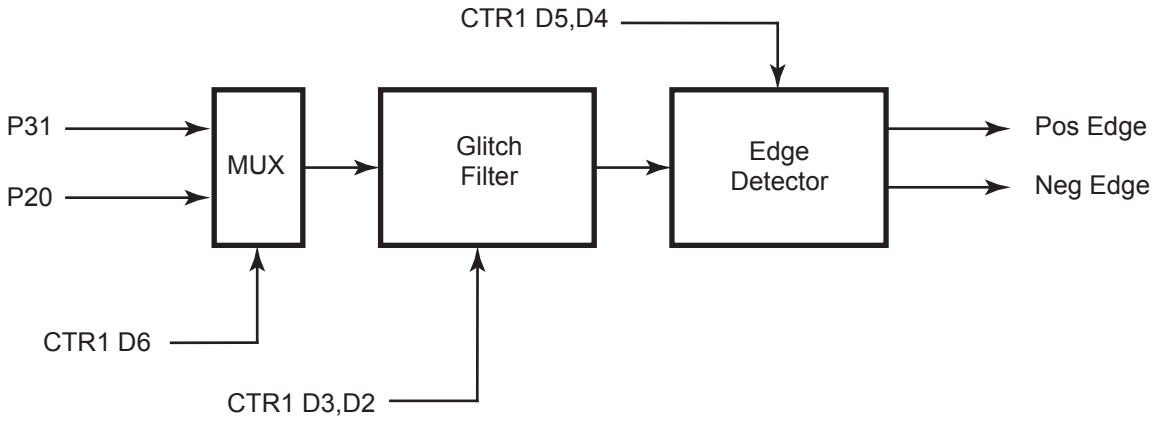


Figure 4. Glitch Filter Circuitry

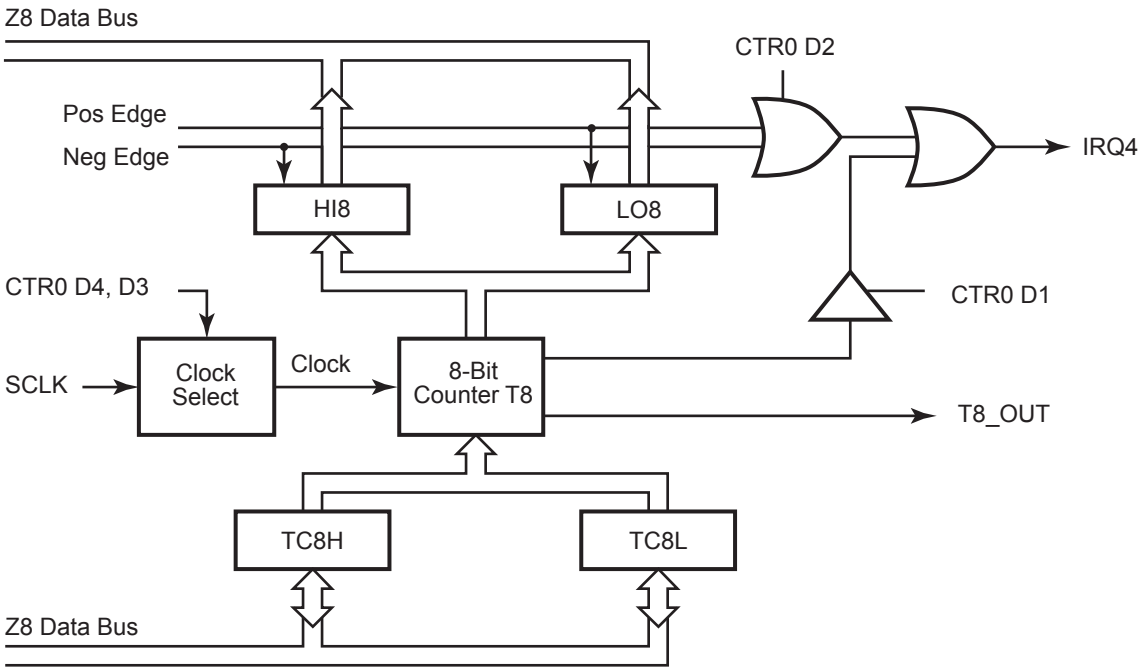


Figure 5. 8-Bit Counter/Timer Circuits

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Positive Edge or Negative Edge line when an edge is detected. Glitches in the input signal which feature a width less than specified (CTR1 D3–D2) are filtered out (Figure 4).

T8 Transmit Mode

When T8 is enabled, the output of T8 depends on CTR1, D1. If CTR1, D1 is 0, T8_OUT is 1. If CTR1, D1 is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE PASS mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0, D5) sets, and a time-out interrupt is generated if it is enabled (CTR0, D1—see Figure 6). In MODULO-N mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), and TC8L is loaded; if T8_OUT is 1, TC8H is loaded. T8

counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0, D5) and generates an interrupt if enabled (CTR0, D1—see Figure 7). This action completes one cycle. T8 then loads from TC8H or TC8L according to the T8_OUT level, and repeats the cycle.

The values in TC8H or TC8L can be modified at any time. The new values take effect when they are loaded. Care must be taken not to write these registers at the time the values are to be loaded into the counter/timer. This step helps to ensure known operation. *An initial count of 1 is not allowed (a nonfunction occurs).* An initial count of 0 causes TC8 to count from 0 to FFh to FEh. A transition from 0 to FFh is not a time-out condition.

Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended. Two successive commands are necessary. First, stop the counter/timers. Second, reset the status bits. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur.

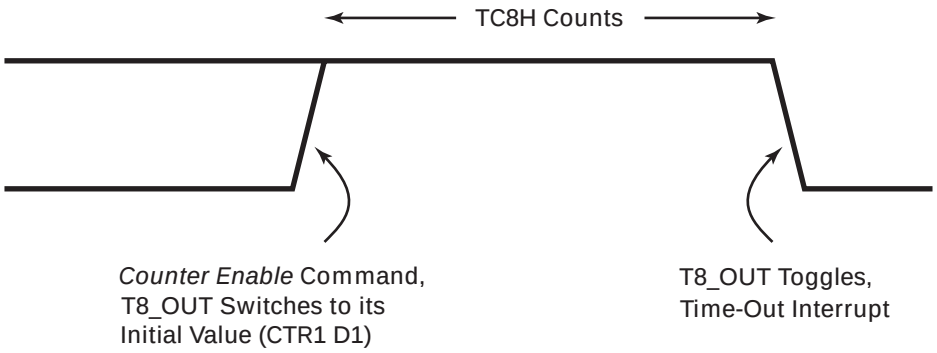


Figure 6. 18_OUT in Single-Pass Mode

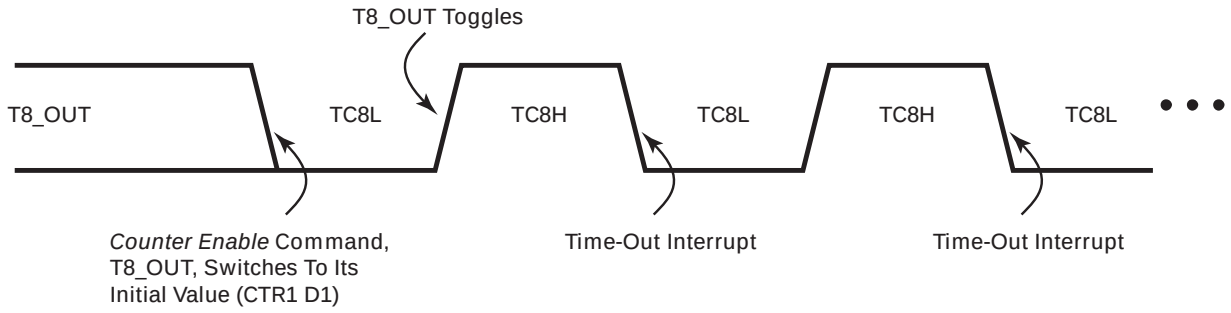


Figure 7. 18_OUT in Modulo-N Mode

T8 Demodulation Mode

Program TC8L and TC8H to register location FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5–D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5–D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if negative edge, HI8. When one of the edge detect status bits (CTR1, D1–D0) is set, an interrupt is generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the time-out status bit (CTR0, D5) sets, an interrupt is generated if enabled (CTR0, D1), and T8 continues counting from FFh (Figure 8).

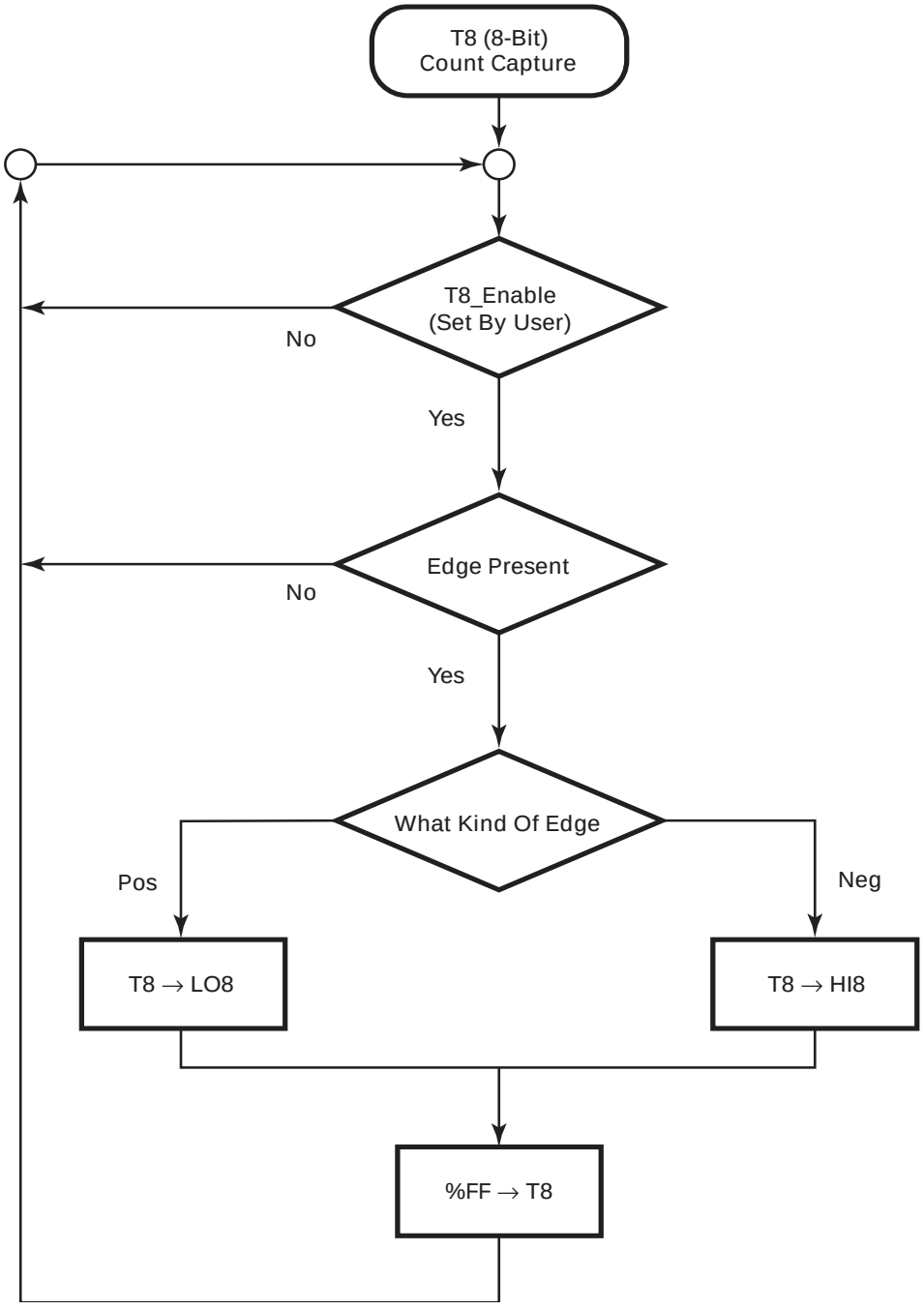


Figure 8. Demodulation Mode Count Capture Flowchart

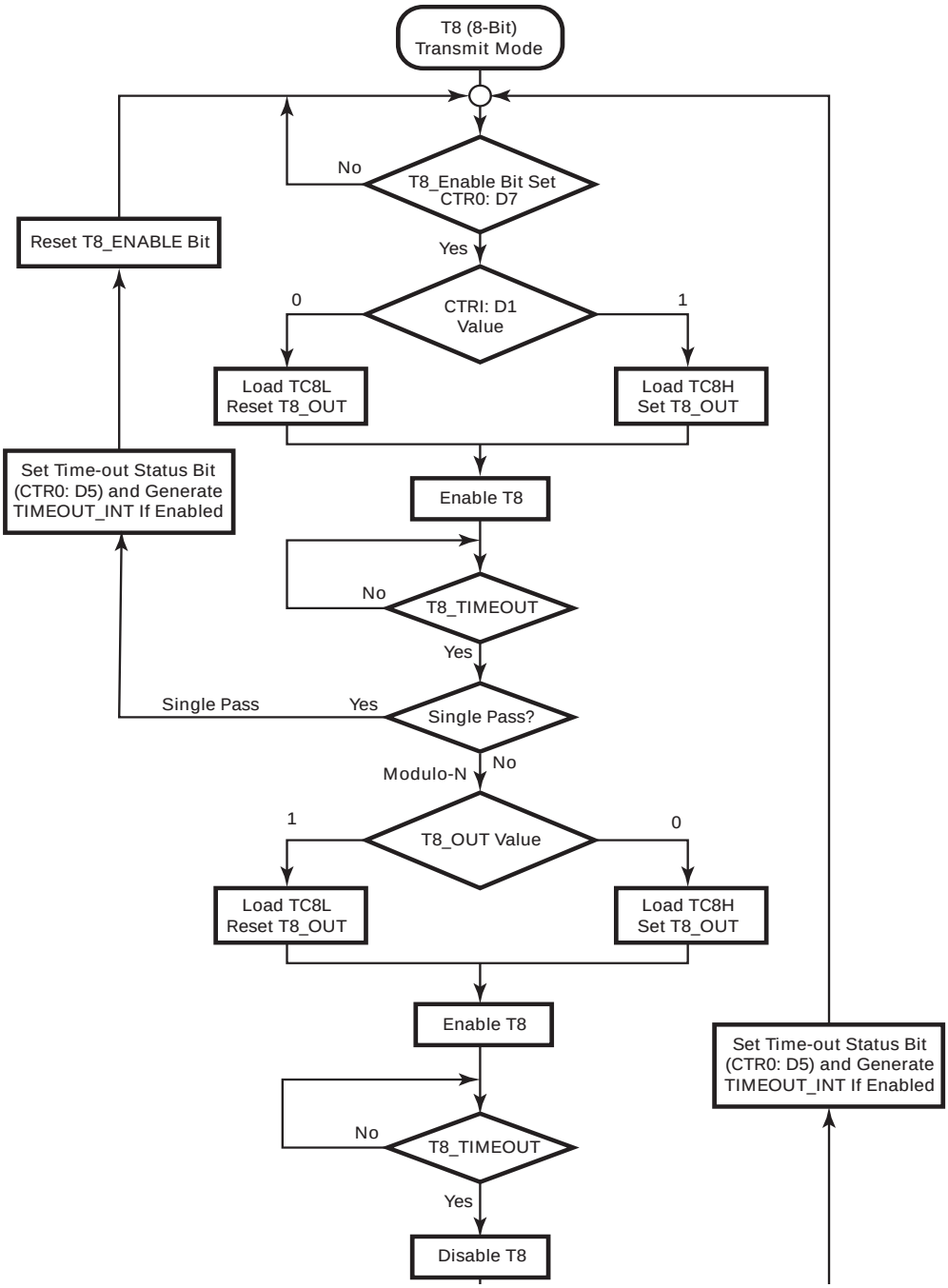


Figure 9. Transmit Mode Flowchart

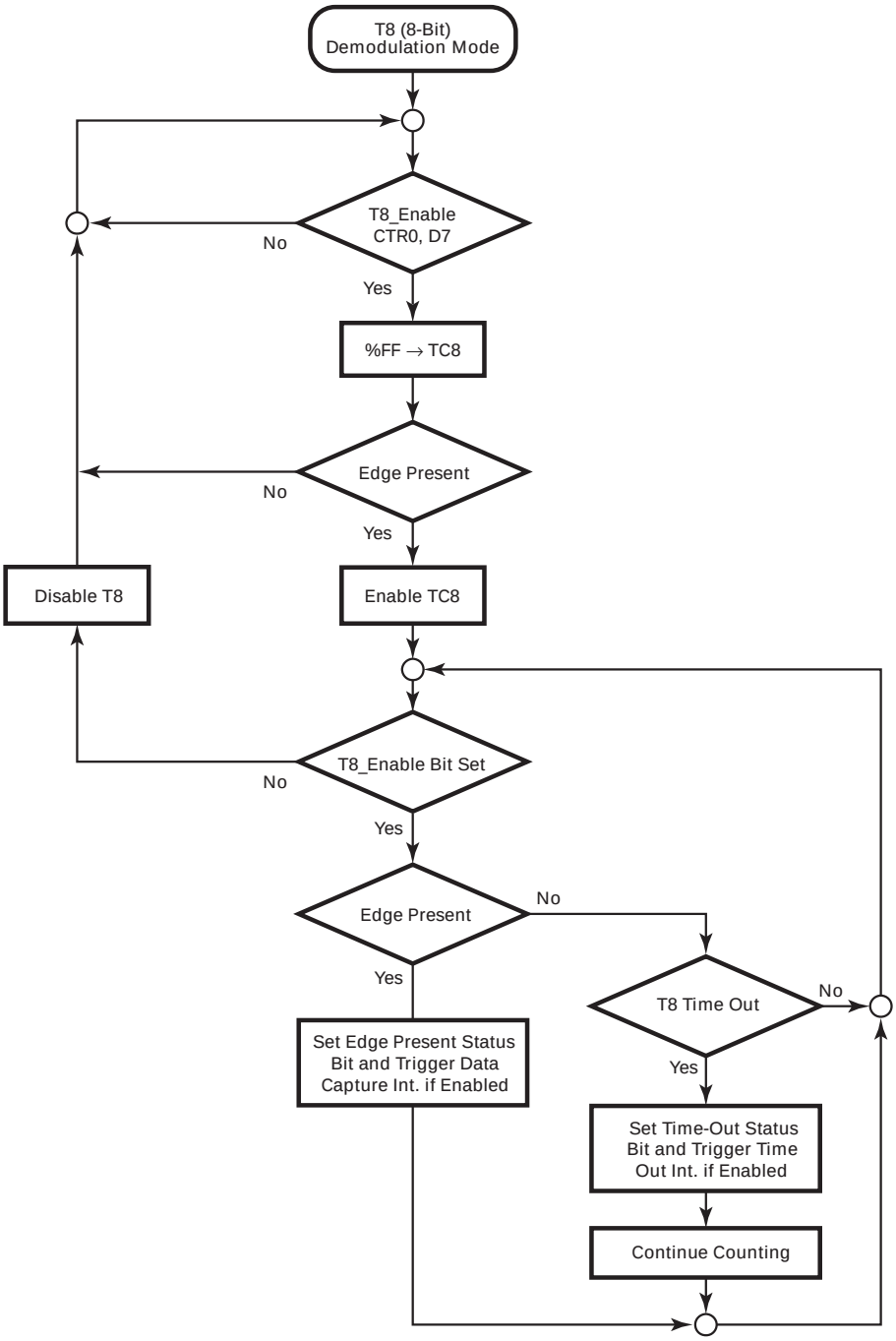


Figure 10. Demodulation Mode Flowchart

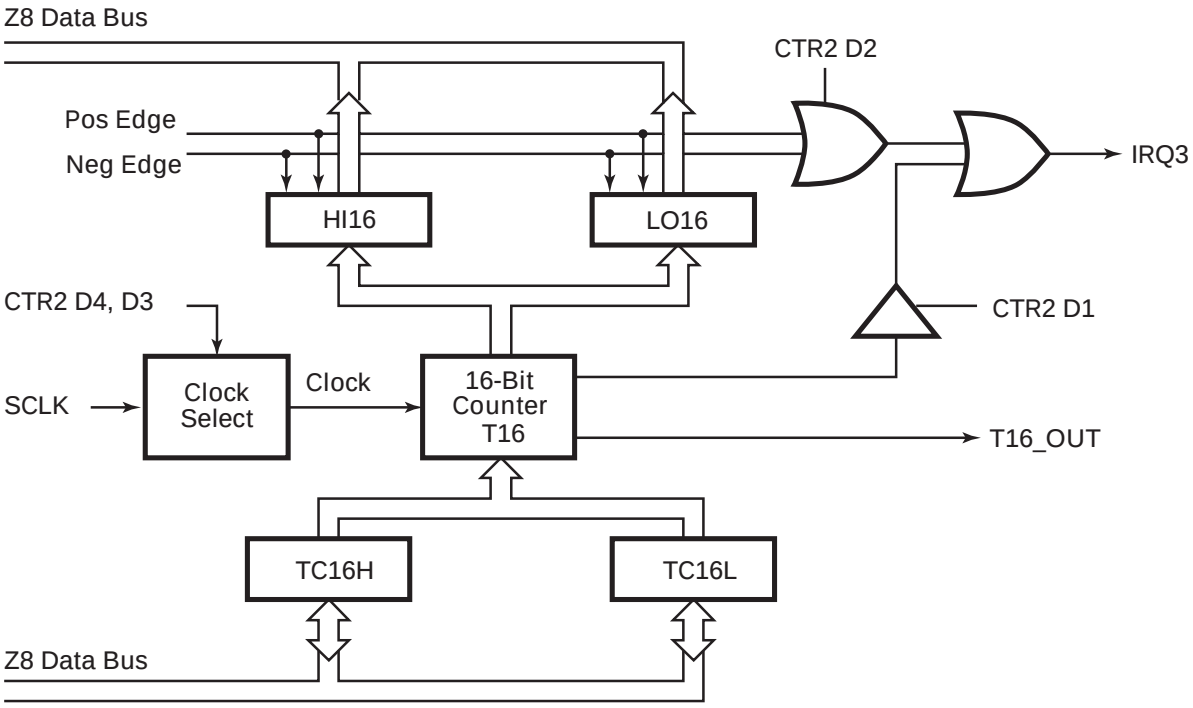


Figure 11. 16-Bit Counter/Timer Circuits

T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled is dependent on CTR1, D0. If CTR1, D0 is a 0, T16_OUT is a 1; if CTR1, D0 is a 1, T16_OUT is 0. Whether enabled or not, the output of T16 can be forced to either a 0 or 1 by programming CTR1, D3–D2) to a 10 or 11.

When T16 is enabled, TC16H x 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong mode), an interrupt is generated if enabled (CTR2, D1), and a status bit (CTR2, D5) is set.

Note: *Global interrupts override this function as described in the interrupts section. If T16 is in SINGLE-PASS mode, it is stopped at this point. If it is in MODULO-N mode, it is loaded with:*

TC16H x 256 + TC16L and the counting continues.

The user can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded. Care must be taken not to load these registers at the time the

values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFh to FFFEh. A transition from 0 to FFFFh is not a time-out condition.

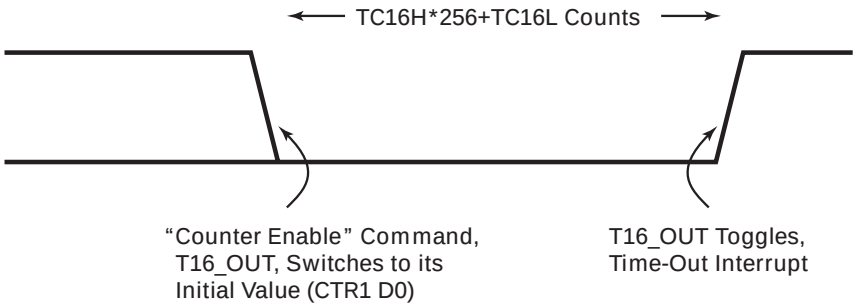


Figure 12. T16_OUT in Single-Pass Mode

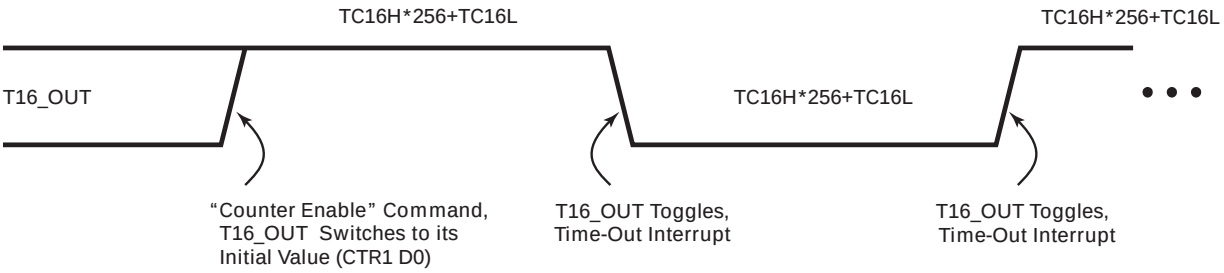


Figure 13. T16_OUT in Modulo-N Mode

T16 Demodulation Mode

The user should program TC16L and TC16H to FFh. After T16 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5–D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 is 0. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current count in T16 is one's complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1 D1, D0) is set and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFh and starts again.

If D6 of CTR2 is 1. T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload, and continues counting.

If the D6 bit of CTR2 is toggled (by writing a 0 and then a 1 to D6), T16 captures and reloads on the next edge (rising, falling, or both, depending on CTR1 D5, D4). However, the D6 bit continues to ignore subsequent edges.

If T16 reaches 0, it continues counting from FFFFh. During that time, a status bit (CTR2, D5) is set and an interrupt time-out is generated if enabled (CTR2, D1).

Ping-Pong Mode

PING-PONG mode is only valid in TRANSMIT mode. T8 and T16 must be programmed in SINGLE PASS mode, CTR0, D6 and CTR2, D6 and Ping-Pong mode must be programmed in CTR1, D3–D2. The user begins the operation by enabling either T8 or T16 (CTR0, D1 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to the value returned by T8_OUT, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16_OUT switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1.

Note: *Enabling Ping-Pong operation while the counter/timers are running may cause intermittent counter/timer function. To avoid this behavior, disable the counter/timers, then reset the status flags prior to instituting the operation.*

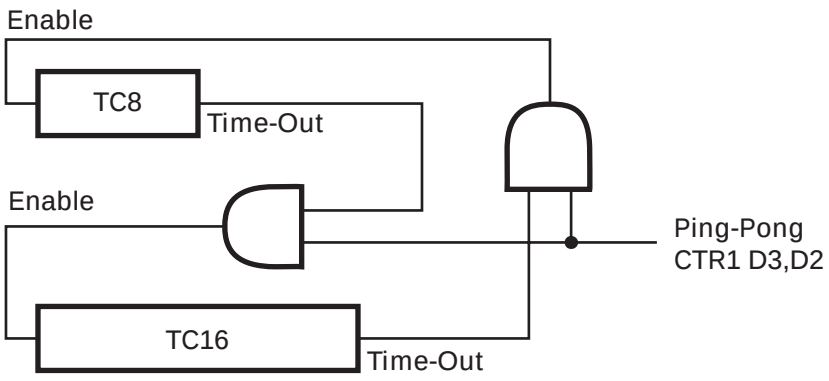


Figure 14. Ping-Pong Mode

Initiating Ping-Pong Mode

First, make sure both counter/timers are not running. From that point, set T8 into SINGLE PASS mode (CTR0, D6), set T16 into SINGLE PASS mode (CTR2, D6), and set PING-PONG mode (CTR1, D2–D3). These instructions are not in any particular sequence. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The time-out bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

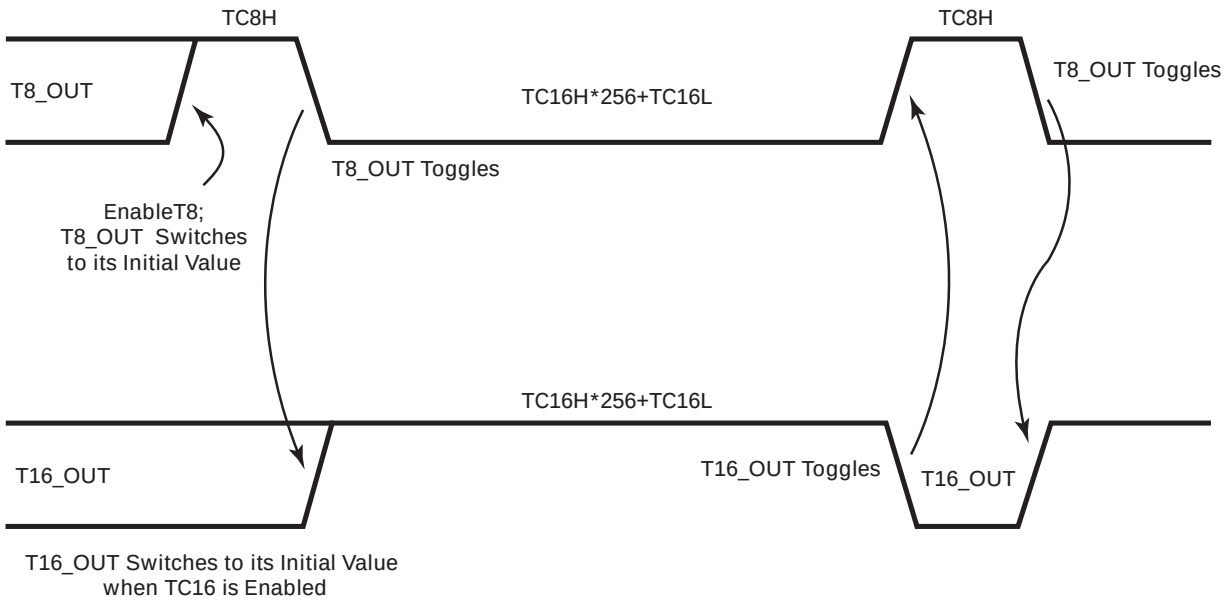


Figure 15. T8_OUT and T16_OUT in Ping-Pong Mode

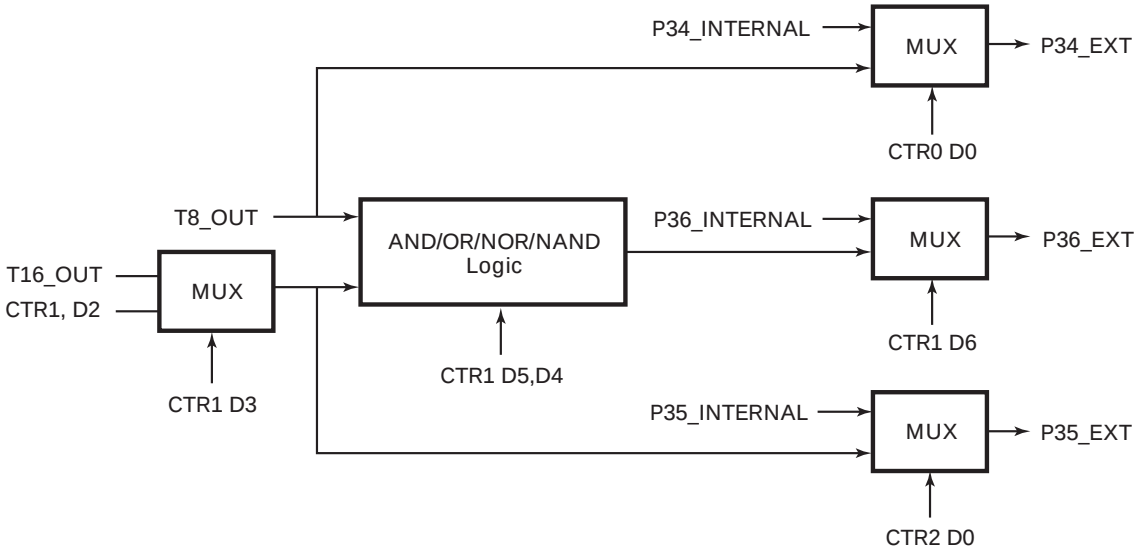


Figure 16. Output Circuit

Control Registers

Z8 Standard Control Registers

Port 2 Mode Register

The Port 2 Mode Register control bits are described in Table 7.

Table 7. Port 2 Mode Register (P2M) R246—F6h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	U	U	U	U	U	U	U	1
Note: W = Write, U = Undefined.								

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D0	P27–P20	W	FFh	P27–P20 0: Defines bit as output 1: Defines bit as input

Port 3 Mode Register

The Port 3 Mode Register control bits are described in Table 8.

Table 8. Port 3 Mode Register (P3M) R247—F7h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	U	U	U	U	U	U	0	0
Note: W = Write, U = Undefined.								

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D6	Reserved	W	U	Reserved; must be 0
D5	Port 3	W	0	**Port 3 I/O** 0: P31 = Input (T_{IN}) P36 = Output (T_{OUT}) 1: P31 = DAV2/$\overline{RDY2}$ P36 = RDY2/$\overline{DAV2}$

Bit Position	Bit Field	R/W	Reset Value	Description
D4–D3	Port 3	W	0	**Port 3 I/O** 00: P33 = Input P34 = Output 01: P33 = Input P34 = $\overline{\text{DM}}$ 10: P33 = Input P34 = $\overline{\text{DM}}$ 11: P33 = $\overline{\text{DAV1}}$/RDY1 P34 = RDY1/$\overline{\text{DAV1}}$
D2	Port 3	W	0	**Port 3 I/O** 0: P32 = Input P35 = $\overline{\text{Output}}$ 1: P32 = $\overline{\text{DAV0}}$/$\overline{\text{RDY0}}$ P35 = RDY0/$\overline{\text{DAV0}}$
D1	Mode	W	0	**Digital/Analog Mode** 0: Digital Mode 1: Analog Mode
D0	Port 2	W	0	**Port 2** 0: Open-Drain 1: Push-Pull

Port 0 and 1 Mode Register

The Port 0 and 1 Mode Register control bits are described in Table 9.

Table 9. Port 0 and 1 Mode Register (P01M) R248—F8h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	U	U	U	0	U	U	0	1
Note: W = Write, U = Undefined.								

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D6	P07–P04	W	UUU0U	**P07–P04 Mode** 00: Output 01: Input* 1X: A15–A12
D5	External Memory Timing	W	U	**External Memory Timing** 0: Normal* 1: Extended
D4–D3	P17–P10	W	00	**P17–P10 Mode** 00: Byte Output 01: Reserved 10: AD7–AD0 11: High-impedance AD7–AD0, AS, DS, R/W, A11–A8, A15–A12, if selected
D2	Stack	W	0	**Stack Selection** 0: External 1: Internal*
D1–D0	P03–P00	W	01	**P03–P00 Mode** 00: Output 01: Input* 1X: A11–A8

Note: * Default setting after reset.

Interrupt Priority Register

The Interrupt Priority Register control bits are described in Table 10.

Table 10. Interrupt Priority Register (IPR) R249—F9h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	U	U	U	U	U	U	U	U
Note: W = Write, U = Undefined.								

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D6	Reserved	W	U	Reserved; must be 0
D5	IRQ3, IRQ5	W	U	**IRQ3, IRQ5 Priority (Group A)** 0: IRQ5 > IRQ3 1: IRQ3 > IRQ5
D4–D3, D0	Interrupt	W	UUU	**Interrupt Group Priority** 000: Reserved 001: C > A > B 010: A > B > C 011: A > C > B 100: B > C > A 101: C > B > A 110: B > A > C 111: Reserved
D2	IRQ0, IRQ2	W	U	**IRQ0, IRQ2 Priority (Group B)** 0: IRQ2 > IRQ0 1: IRQ0 > IRQ2
D1	IRQ1, IRQ4	W	U	**IRQ1, IRQ4 Priority (Group C)** 0: IRQ1 > IRQ4 1: IRQ4 > IRQ1

Interrupt Request Register

The Interrupt Request Register control bits are described in Table 11.

Table 11. Interrupt Request Register (IRR) R250—FAh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D6	Interrupt Edge	R/W	00	**Interrupt Edge** P31↓ P32↓ = 00 P31↓ P32↑ = 01 P31↑ P32↓ = 10 P31↑ P32↑↓ = 11
D5	Reserved	W	U	Reserved; must be 0
D4–D0	Interrupt Requests	R/W	00000	**Interrupt Requests** IRQ0 = P32 Input IRQ1 = P33 Input IRQ2 = P31 Input IRQ3 = T16 IRQ4 = T8

Interrupt Mask Register

The Interrupt Mask Register control bits are described in Table 12.

Table 12. Interrupt Mask Register (IMR) R251—FBh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset Value	Description
D7	Interrupts	R/W	0	**Interrupts** 0: Master Interrupt Disable 1: Master Interrupt Enable
D6–D5	Reserved	R/W	0	Reserved; must be 0
D4–D0	Interrupt Requests	R/W	00000	**Interrupt Requests** 0: 1: Enables IRQ4–IRQ0 (D0 = IRQ0)

Flag Register

The Flag Register control bits are described in Table 13.

Table 13. Flag Register (Flags) R252—FCh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	U	U	U	U	U	U	U	U
Note: R = Read. W = Write, U = Undefined.								

Bit Position	Bit Field	R/W	Reset Value	Description
D7	Carry	R/W	U	Carry Flag
D6	Zero	R/W	U	Zero Flag
D5	Sign	R/W	U	Sign Flag
D4	Overflow	R/W	U	Overflow Flag
D3	Decimal Adjust	R/W	U	Decimal Adjust Flag
D2	Half Carry	R/W	U	Half Carry

Bit Position	Bit Field	R/W	Reset Value	Description
D1	User F2	R/W	U	User Flag F2
D0	User F1	R/W	U	User Flag F1

Register Pointer

The Register Pointer control bits are described in Table 14.

Table 14. Register Pointer (RP) R253—FDh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D4	Expanded Register	R/W	0000	Expanded Register Bank Pointer*
D3–D0	Working Register	R/W	0000	Working Register Pointer*

Note: *Default setting after reset = 0000 0000.

Stack Pointer

The Stack Pointer control bits are described in Table 15.

Table 15. Stack Pointer (SP) R255—FFh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Note: R = Read, W = Write.								

Bit Position	Bit Field	R/W	Reset Value	Description
D7–D0	Stack Pointer	R/W	00h	Stack Pointer (SP7–SP0)

Stop Mode Recovery Control Registers

The device allows 16 individual I/O pins (Ports 2 and 5) to be used as a Stop Mode Recovery sources. STOP mode is exited when one of these SMR sources is toggled.

Stop Mode Recovery Register. The SMR register serves two functions. Bit D7 of the SMR register, as indicated in Table 16., is the Stop-Mode Flag that is set upon entering STOP mode. A 0 in this bit indicates that the device is reset by a POR or WDT Reset. A POR or WDT Reset is sometimes referred to as a *cold start*. A 1 in bit D7 indicates that the device was awakened by a SMR source. Waking a device with a SMR source is sometimes referred to as a *warm start*.

Table 16. Stop Mode Recovery Register—SMR 0Bh/R11 Bank 0Fh: READ/WRITE

Bit	7	6	5	4	3	2	1	0
Bit/Field	Stop Flag	Reserved	Stop Delay	Reserved			SCLK Select	
R/W	R	R/W	W	R/W	R/W	R/W	W	W
Reset State	0	0	1	0	0	0	0	0

Note: R = Read, W = Write, X = Indeterminate.

Bit Position	Bit/Field	R/W	State	Description
7	Stop-Mode Flag	R	1	Stop Recovery (warm start)
			0	POR/WDT Reset (cold start)
		W	X	No Effect
6	Reserved	R	1	Always reads 1
		W	X	No Effect
5	Stop Delay	R	1	Always reads 1
		W	1	Enable 5ms $\overline{\text{Reset}}$ delay
			0	Disable $\overline{\text{Reset}}$ delay after SMR
4–2	Reserved	R	1	Always reads 111
		W	X	No Effect
1–0	System Clock Select	R	11	Always reads 11
		W	11	SCLK, TCLK = XTAL ÷ 16
			10	SCLK, TCLK = XTAL
			01	SCLK, TCLK = XTAL ÷ 32
			00	SCLK, TCLK = XTAL ÷ 2

The second function of the SMR register is the selection of the external clock divide value. The purpose of this control is to selectively reduce device power

consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

Port 2 Stop Mode Recovery. The P2SMR register, Table 17., defines which I/O lines in Port 2 are to be used as Stop Mode Recovery sources.

Table 17. Port 2 Stop Mode Recovery Register—P2SMR 01h/R1 Bank 0Fh: READ/WRITE

Bit	7	6	5	4	3	2	1	0
Bit/Field	P27RS	P26RS	P25RS	P24RS	P23RS	P22RS	P21RS	P20RS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset State	0	0	0	0	0	0	0	0

Note: R = Read, W = Write.

Bit Position	Bit/Field	R/W	State	Description
7–0	Port 2 Stop Mode Recovery	R/W	1	Recovery source
			0	Not a recovery source

Watchdog Timer

Watchdog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an onboard RC oscillator or external oscillator from the X_{IN} pin. The POR clock source is selected with bit 4 of the WDT register (Table 18.).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within the first 64 internal system clocks. After that, the WDTMR is WRITE-protected.

Note: *WDT time-out while in STOP mode does not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but the POR delay counter is still enabled even though the SMR stop delay is disabled.*

Table 18. Watchdog Timer Mode Register—WDTMR 0Fh/R15: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	1	1	0	1

Note: R = Read, W = Write, X = Indeterminate.

Bit/ Field	Bit Position	R/W	State	Description
D7–D5	Reserved	W	X	Reserved—must be 0
D4	X_{IN}	W	0	**XIN/INT RC Select for WDT** 0: On-Board RC 1: Crystal
D3	WDT	W	1	WDT During STOP
D2	WDT	W	1	WDT During HALT
D1–D0	WDT Tap	W	01	**WDT Tap Int RC OSC System Clock** 00: 3.5 ms 128 SCLK 01: 10.0 ms 256 SCLK 10: 14.0 ms 512 SCLK 11: 56.0 ms 2048 SCLK

Note: Not used in conjunction with SMR Source.

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65º	+150º	C
T_A	Operating Ambient Temperature		†	C

Notes:
*Voltage on all pins with respect to GND.
†See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

DC Characteristics

Table 19. DC Characteristics

			T_A = 0°C to +70°C T_{A2} = –40°C to +105°C					
Sym	Parameter	V_{CC}	Min	Max	Typ @ 25°C[1]	Units	Conditions	Notes
	Max Input Voltage	4.5V		7		V	I_{IN} <250 µA	
		5.5V		7		V	I_{IN} <250 µA	
V_{CH}	Clock Input High Voltage	4.5V	0.9 V_{CC}	V_{CC}+0.3		V	Driven by External Clock Generator	
		5.5V	0.9 V_{CC}	V_{CC}+0.3		V		
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}		V		
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	0.5Vcc	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.5Vcc	V		

Table 19. DC Characteristics (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C, T_{A2} = –40°C to +105°C Min	Max	Typ @ 25°C[1]	Units	Conditions	Notes
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	0.5Vcc	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	0.5Vcc	V		
V_{OH1}	Output High Voltage	4.5V	V_{CC}–0.4		4.9	V	I_{OH} = –0.5 mA	
		5.5V	V_{CC}–0.4		4.9	V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37)	4.5V	V_{CC}–0.8V			V	I_{OH} = –7.0 mA	
		5.5V	V_{CC}–0.8V			V	I_{OH} = –7.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = 4.0 mA	
		5.5V		0.4	0.2	V	I_{OL} = 4.0 mA	
V_{OL2}	Output Low Voltage	4.5V		0.8	0.3	V	I_{OL} = 7.0 mA	2
		5.5 V		0.8	0.4	V	I_{OL} = 7.0 mA	2
V_{OL2}	Output Low Voltage (P00, P01, P36,P37)	4.5V		0.8	0.3	V	I_{OL} = 10.0 mA	
		5.5V		0.8	0.2	V	I_{OL} = 10.0 mA	
V_{RH}	Reset Input High Voltage	4.5V	0.8 V_{CC}	V_{CC}	2.5	V		
		5.5V	0.8 V_{CC}	V_{CC}	3.0	V		
V_{RI}	Reset Input Low Voltage	4.5V	V_{SS}–0.3V	0.2 V_{CC}	0.5			
		5.5V	V_{SS}–0.3V	0.2 V_{CC}	0.9			
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage	4.5V	0	V_{CC}–1.0V		V		3
		5.5V	0	V_{CC}–1.0V		V		3
I_{IL}	Input Leakage	4.5V	–1	1	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	1	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1	1	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1	1	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V		–500		µA	V_{IN} = 0V, V_{CC}	
		5.5V		–800		µA	V_{IN} = 0V, V_{CC}	

Table 19. DC Characteristics (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C, T_{A2} = –40°C to +105°C Min	Max	Typ @ 25°C[1]	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		20	16	mA	@16.0 MHz	4,5
		5.5V		30	16	mA	@16.0 MHz	4,5
I_{CC1}	HALT Mode Current (WDT Off)	4.5V		6	2	mA	V_{IN} = 0V, V_{CC} @ 8.0 MHz	4,5
		5.5V		8	5	mA	V_{IN} = 0V, V_{CC} @ 8.0 MHz	4,5
		4.5V		5	1.0	mA	Clock Divide-by-16 @ 8.0 MHz	4
		5.5V		7	3.0	mA	Clock Divide-by-16 @ 8.0 MHz	4
I_{CC2}	STOP Mode Current	4.5V		8	2	µA	V_{IN} = 0V, V_{CC} WDT is off	6,7
		5.5V		10	3	µA	V_{IN} = 0V, V_{CC} WDT is off	6,7
		4.5V		500	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	6,7
		5.5V		800	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	6,7
T_{POR}	Power-On Reset	4.5V	0.5	10	2.0	ms		8
		5.5V	0.5	10	2.0	ms		8
V_{RAM}	Static RAM Data Retention Voltage	V_{RAM}	1.0		0.7	V		9
V_{LV}	V_{CC} Low-Voltage Protection		2.2	2.8	2.6	V		10

Table 19. DC Characteristics (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C, T_{A2} = –40°C to +105°C Min	Max	Typ @ 25°C[1]	Units	Conditions	Notes
R_{PUT}	Pull-up transistor resistance	4.5V			100K	Ohms	V_{IN} = 0_V	11
		5.5V			100K	Ohms	V_{IN} = 0_V	11

Notes:
1. V_{CC} = 5.0V.
2. All outputs excluding P00, P01, P36, and P37.
3. For analog comparator inputs in analog mode.
4. All outputs unloaded; inputs at rail.
5. SCLK = CRYSTAL ÷ 2 mode.
6. Same as note 4, except inputs at $V_{CC.}$
7. Oscillator stopped.
8. Using on-board RC oscillator.
9. Oscillator stops when V_{CC} falls below V_{LV} limit.
10. The V_{LV} increases as the temperature decreases.
11. Weak pull-up transistor option enabled.

AC Characteristics

External I/O or Memory READ/WRITE Timing

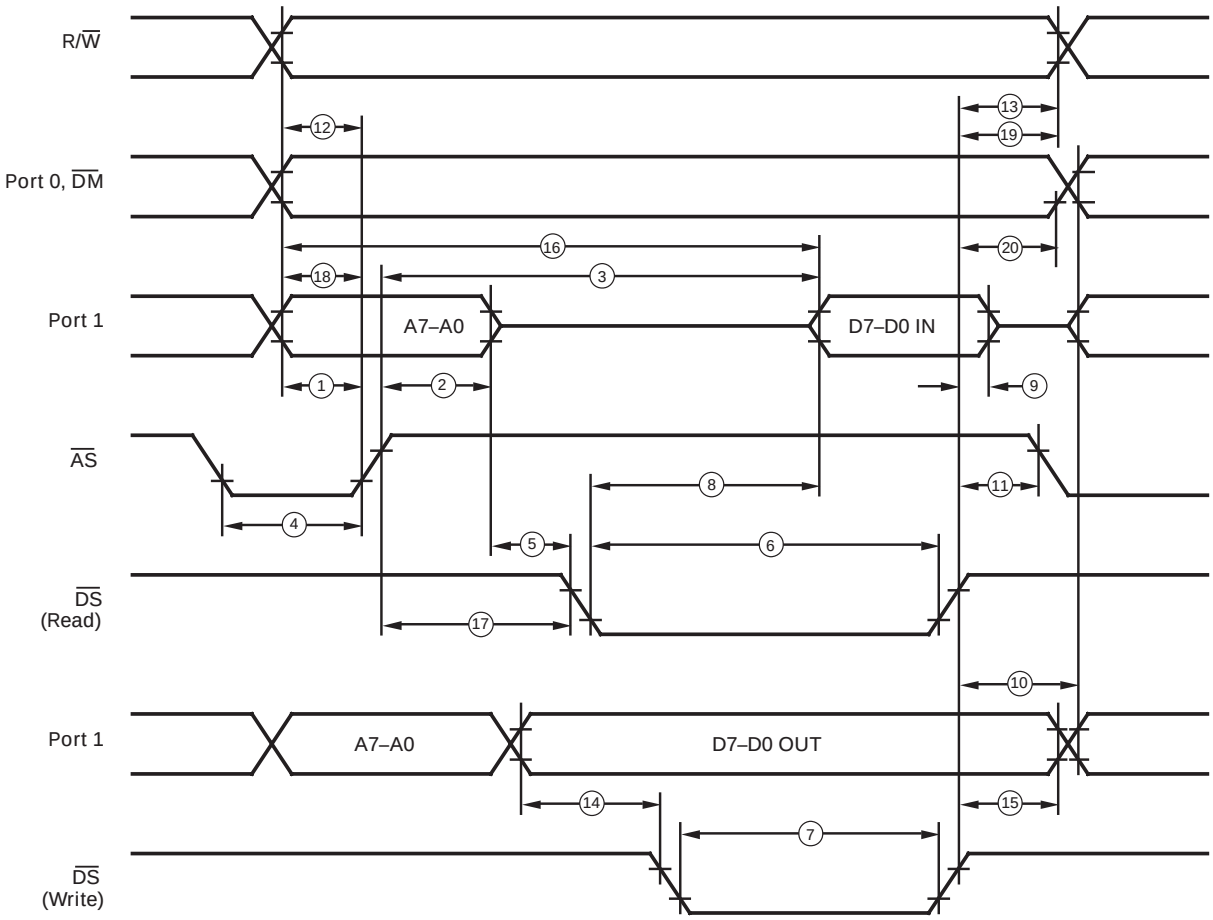


Figure 17. External I/O or Memory READ/WRITE Timing

Table 20. External I/O or Memory Read and Write Timing

				T_A = 0°C to +70°C T_{A2} = –40°C to +105°C						
				12.0 MHz		16.0 MHz				
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_DA(AS)	Address Valid to $\overline{AS}$ Rising Delay	4.5V	35		25		ns	2
			5.5V	35		25		ns	2
2	T_DAS(A)	$\overline{AS}$ Rising to Address Float Delay	4.5V	45		35		ns	2
			5.5V	45		35		ns	2
3	T_DAS(DR)	$\overline{AS}$ Rising to Read Data Required Valid	4.5V		250		180	ns	1,2
			5.5V		250		180	ns	1,2
4	T_WAS	$\overline{AS}$ Low Width	4.5V	55		40		ns	2
			5.5V	55		40		ns	2
5	T_DAz(DS)	Address Float to $\overline{DS}$ Falling	4.5V	0		0		ns	2
			5.5V	0		0		ns	2
6	T_WDSR	$\overline{DS}$ (Read) Low Width	4.5V	200		135		ns	1,2
			5.5V	200		135		ns	1,2
7	T_WDSW	$\overline{DS}$ (Write) Low Width	4.5V	110		80		ns	1,2
			5.5V	110		80		ns	1,2
8	T_DDSR(DR)	$\overline{DS}$ Falling to Read Data Required Valid	4.5V		150		75	ns	1,2
			5.5V		150		75	ns	1,2
9	T_HDR(DS)	Read Data to $\overline{DS}$ Rising Hold Time	4.5V	0		0		ns	2
			5.5V	0		0		ns	2
10	T_DDS(A)	$\overline{DS}$ Rising to Address Active Delay	4.5V	45		50		ns	2
			5.5V	55		50		ns	2
11	T_DDS(AS)	$\overline{DS}$ Rising to $\overline{AS}$	4.5V	30		35		ns	2
			5.5V	45		35		ns	2
12	T_DR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$ Rising Delay	4.5V	45		25		ns	2
			5.5V	45		25		ns	2
13	T_DDS(R/W)	$\overline{DS}$ Rising to R/$\overline{W}$ Not Valid	4.5V	45		35		ns	2
			5.5V	45		35		ns	2

Table 20. External I/O or Memory Read and Write Timing (Continued)

				T_A = 0°C to +70°C T_{A2} = –40°C to +105°C					
				12.0 MHz		16.0 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
14	T_DDW(DSW)	Write Data Valid to $\overline{DS}$ Falling (Write) Delay	4.5V	55		25		ns	2
			5.5V	55		25		ns	2
15	T_DDS(DW)	$\overline{DS}$ Rising to Write Data Not Valid Delay	4.5V	45		35		ns	2
			5.5V	45		35		ns	2
16	T_DA(DR)	Address Valid to Read Data Required Valid	4.5V		310		230	ns	1,2
			5.5V		310		230	ns	1,2
17	T_DAS(DS)	$\overline{AS}$ Rising to $\overline{DS}$ Falling Delay	4.5V	65		45		ns	2
			5.5V	65		45		ns	2
18	T_DDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Falling Delay	4.5V	35		30		ns	2
			5.5V	35		30		ns	2
19	T_DDS(DM)	$\overline{DS}$ Rise to $\overline{DM}$ Valid Delay	4.5V	45		35		ns	2
			5.5V	45		35		ns	2
20	T_HDS(A)	$\overline{DS}$ Rise to Address Valid Hold Time	4.5V	45		35		ns	2
			5.5V	45		35		ns	2

Notes:
1. When using extended memory timing, add 2 TpC.
2. Timing numbers provided are for minimum TpC.

Standard Test Load

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

Additional Timing

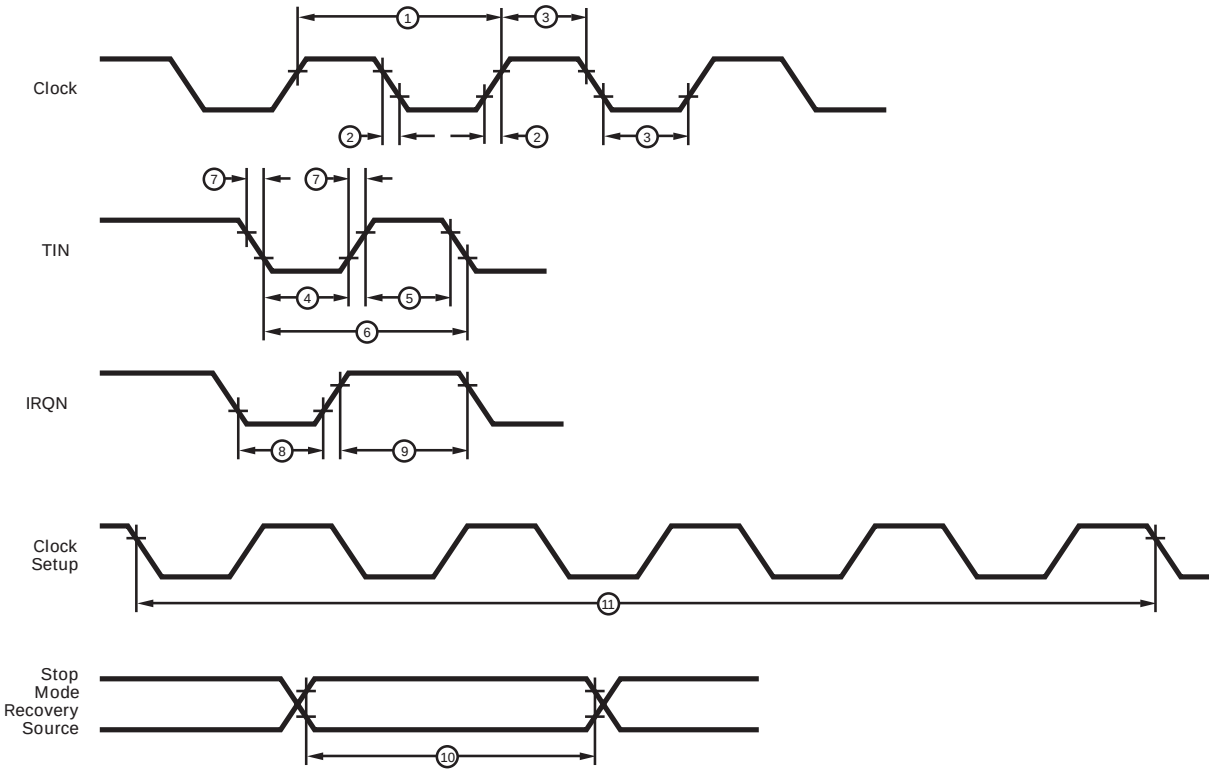


Figure 18. Additional Timing

Table 21. Additional Timing

				T_A = 0°C to +70°C						
				12 MHz		16 MHz				
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	T_PC	Input Clock Period	4.5V	83	DC	63	DC	ns	1
			5.5V	83	DC	63	DC	ns	1
2	T_RC, T_FC	Clock Input Rise and Fall Times	4.5V		15		15	ns	1
			5.5V		15		15	ns	1
3	T_WC	Input Clock Width	4.5V	41		31		ns	1
			5.5V	41		31		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	4.5V	100		100		ns	1
			5.5V	70		70		ns	1

Table 21. Additional Timing (Continued)

				T_A = 0°C to +70°C					
				12 MHz		16 MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
5	$T_WT_{IN}H$	Timer Input High Width	4.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	T_PT_{IN}	Timer Input Period	4.5V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	T_RT_{IN}, T_FT_{IN}	Timer Input Rise	4.5V		100		100	ns	1
			5.5V		100		100	ns	1
8	T_WIL	Interrupt Request Low Time	4.5V	100		70		ns	1,2
			5.5V	70		70		ns	1,2
9	T_WIH	Interrupt Request Input High Time	4.5V	5TpC		5TpC			1,2
			5.5V	5TpC		5TpC			1,2
10	T_{WSM}	Stop Mode Recovery Width Spec	4.5V	12		12		ns	3
			5.5V	12		12		ns	3
						12			4
						12			4
11	T_{OST}	Oscillator Start-up Time	4.5V		5TpC		5TpC		4
			5.5V		5TpC		5TpC		4

Table 21. Additional Timing (Continued)

No	Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
12	T_{WDT}	Watchdog Timer Delay Time	4.5V	2.0		2.0		ms	5,6,7
			5.5V	2.0		2.0		ms	5,6,7
			4.5V	4.0		4.0		ms	5,6,8
			5.5V	4.0		4.0		ms	5,6,8
			4.5V	8.0		8.0		ms	5,6,9
			5.5V	8.0		8.0		ms	5,6,9
			4.5V	32		32		ms	5,6,10
			5.5V	32		32		ms	5,6,10

Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Reg. SMR bit D5 = 1.
4. Reg. SMR bit D5 = 0.
5. WDT Bit D4 = 0.
6. Reg. WDTMR.
7. Reg. WDTMR bit D1 = 0, D0 = 0.
8. Reg. WDTMR bit D1 = 0, D0 = 1.
9. Reg. WDTMR bit D1 = 1, D0 = 0.
10. Reg. WDTMR bit D1 = 1, D0 = 1.

Handshake Timing

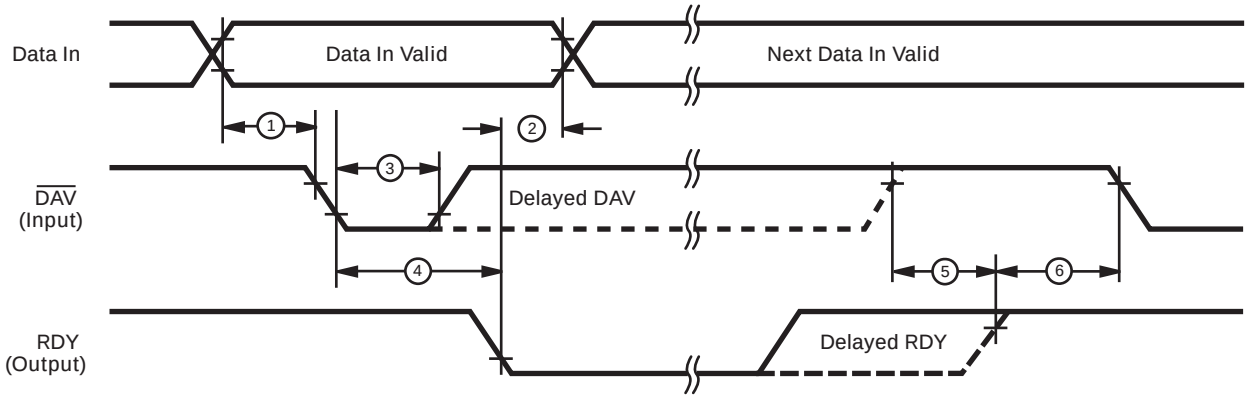


Figure 19.Port I/O with Output Handshake Timing

Figure 20. Port I/O with Output Handshake Timing

Table 22. Handshake Timing

				T_A = 0°C to +70°C T_A = –40°C to +105°C				
				12 MHz		16 MHz		Data
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Direction
1	TSDi(DAV)	Data in Setup Time	4.5V	0		0		Input
			5.5V	0		0		Input
2	ThDi(DAV)	Data in Hold Time	4.5V	160		160		Input
			5.5V	115		115		Input
3	TwDAV	Data Available Width	4.5V	155		155		Input
			5.5V	110		110		Input
4	TdDAVlf(RDY)	DAV Falling to RDY Falling Delay	4.5V		160		160	Input
			5.5V		115		115	Input
5	TdDAVlr(RDY)	DAV Rising to RDY Falling Delay	4.5V		120		120	Input
			5.5V		80		80	Input
6	TdRDYlr(DAV)	RDY Rising to DAV Falling Delay	4.5V	0		0		Input
			5.5V	0		0		Input
7	TdDO(DAV)	Data Out to DAV Falling Delay	4.5V	31		31		Output
			5.5V	31		31		Output
8	TdDAVOf(RDY)	DAV Falling to RDY Falling Delay	4.5V	0		0		Output
			5.5V	0		0		Output
9	TdRDYOf(DAV)	RDY Falling to DAV Rising Delay	4.5V		160		160	Output
			5.5V		115		115	Output
10	TwRDY	RDY Width	4.5V	110		110		Output
			5.5V	80		80		Output
11	TdRDYOr(DAV)	RDY Rising to DAV Falling Delay	4.5V		110		110	Output
			5.5V		80		80	Output

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin Figure 21.

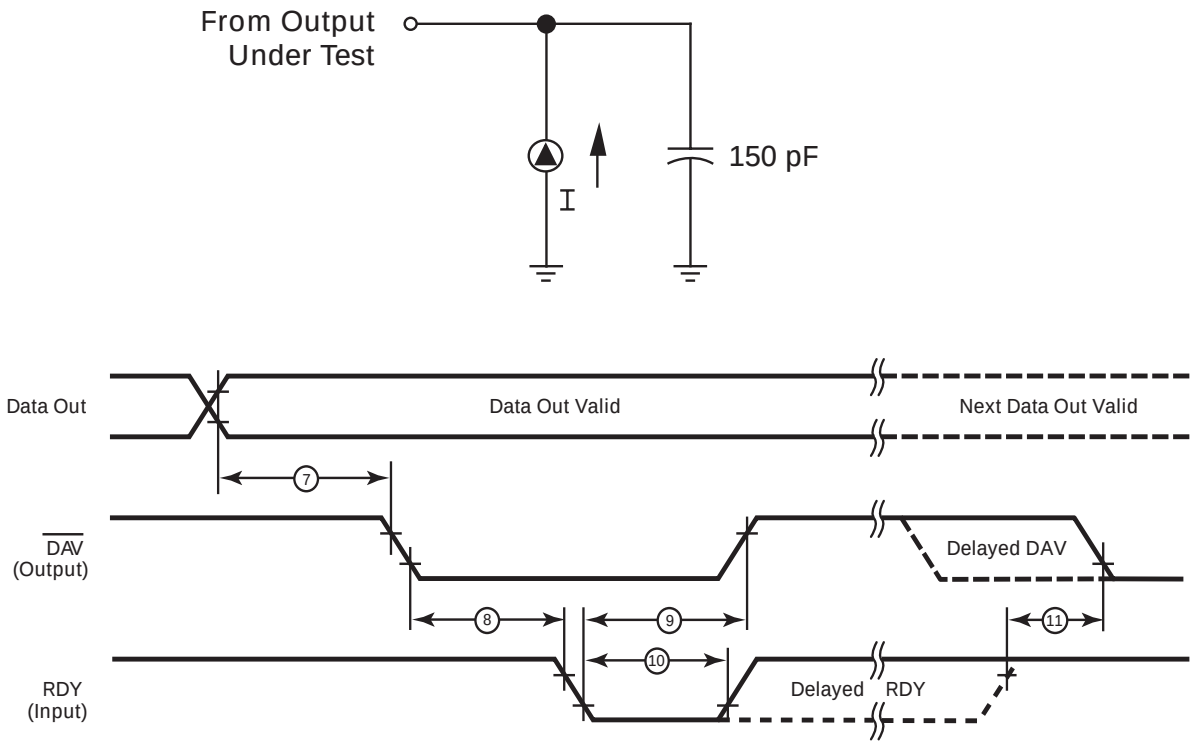


Figure 21. Test Load Diagram

Capacitance

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

Pin Functions

$\overline{DS}$ (Output, active Low). Data Strobe is activated one time for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{DS}$. For WRITE operations, the falling edge of $\overline{DS}$ indicates that output data is valid. Under program control, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, Port 0, and Port 1 can be placed in the high-impedance state.

$\overline{AS}$ (Output, active Low). Address Strobe is pulsed one time at the beginning of each machine cycle for each external memory transfer. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{AS}$. Under program control, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, Port 0, and Port 1 can be placed in the high-impedance state.

X_{IN} Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or an external single-phase clock to the on-chip oscillator input.

X_{OUT} Crystal 2 (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

R/$\overline{W}$ READ/WRITE (output, write Low). The R/$\overline{W}$ signal is Low when writing to the external program or data memory. Under program control, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, Port 0, and Port 1 can be placed in the high-impedance state.

Port 0 (P07–P00). Port 0 is an 8-bit (bidirectional) CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control $\overline{DAV0}$ and RDY0. Handshake signal direction is dictated by the I/O direction to Port 0 of the upper nibble, P07–P04. The lower nibble must flow in the same direction as the upper nibble.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O, while the lower nibble is used for addressing. If one or both nibbles are required for I/O operation, each must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

Port 0 is set in the HIGH IMPEDANCE mode (if selected as an address output) along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ through P01M bits D4 and D3 (Figure 1).

An optional 100 KΩ pull-up is available as a mask option on all Port 0 bits with nibble select. These pull-ups are disabled when configured (bit by bit) as an output.

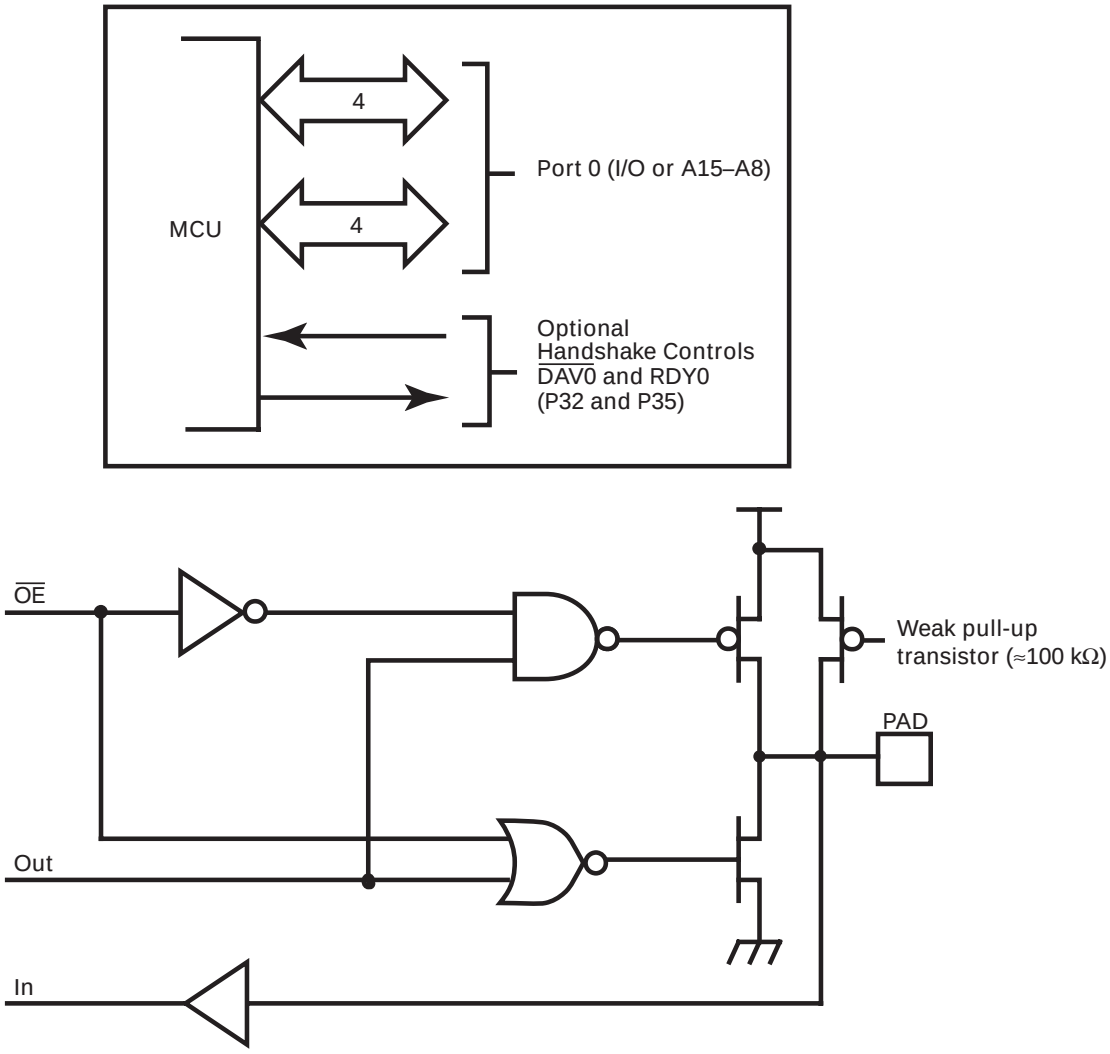


Figure 1. Port 0 Configuration

Port 1 (P17–P10). Port 1 is a multiplexed Address (A7–A0) and Data (D7–D0), CMOS-compatible port. Port 1 is dedicated to the Zilog ZBus®-compatible memory interface. Port 1 operations are supported by the Address Strobe ($\overline{AS}$) and Data Strobe ($\overline{DS}$) lines, and by the READ/WRITE (R/$\overline{W}$) and Data Memory ($\overline{DM}$) control lines. Data memory READ/WRITE operations are done through this port (Figure 2). If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86C72 to share common resources in multiprocessor and DMA applications. Port1 can also be configured for standard port output mode.

The autolatches are hardware-enabled on Port I/O. The input trip point for detecting a high or low input level is set at $V_{CC} \div 2$.

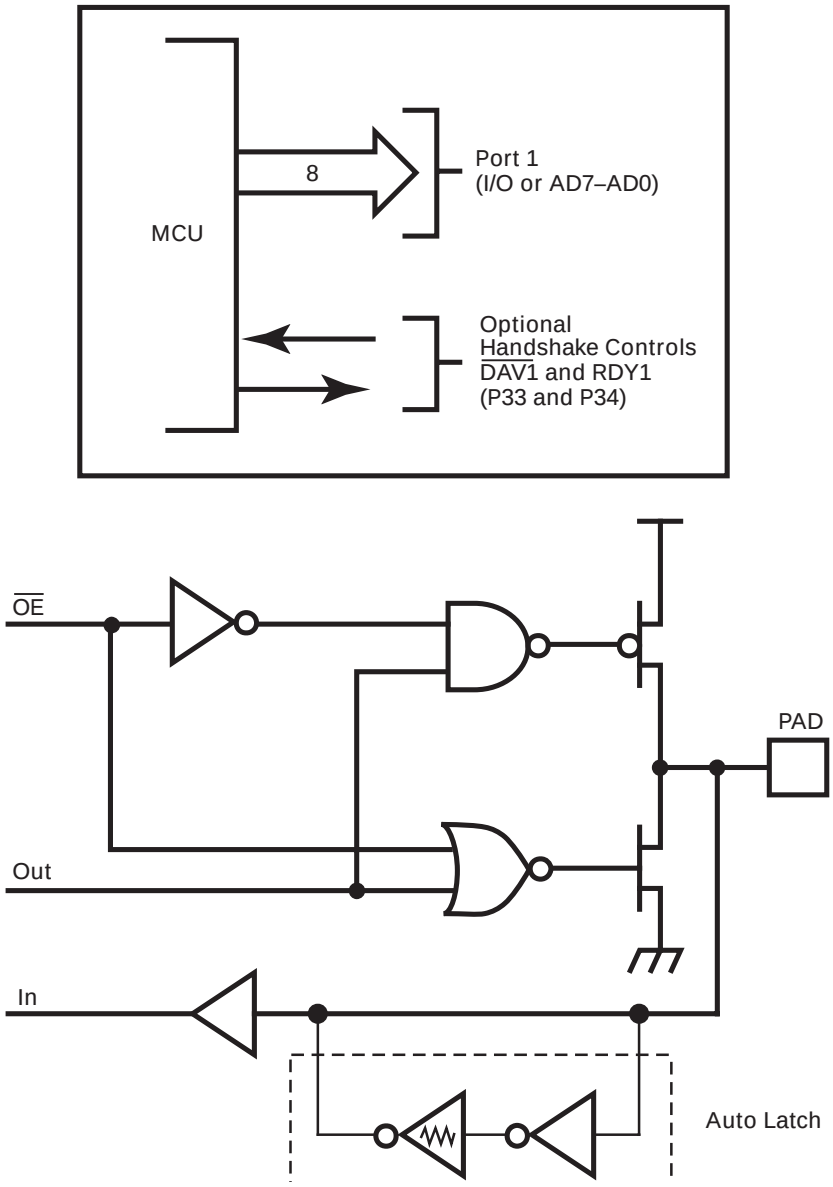


Figure 2. Port 1 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit (bidirectional) CMOS- compatible I/O port. These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight 100 KΩ (±50%) pull-up resistors on this port.
Bits programmed as outputs are globally programmed as either push-pull or open-drain. Port 2 may be placed under handshake control. In this configuration, Port 3 lines (P31 and P36) are used as the handshake controls lines $\overline{\text{DAV2}}$ and RDY2. The handshake signal assignment for Port 3 (lines P31 and P36) is dictated by the direction (input or output) assigned to Bit 7, Port 2 (Figure 3). The eight bits of Port 2 are configured as inputs with open-drain outputs.

Port 2 also features an 8-bit input NOR and a NAND gate, which can be used to wake up the part. P20 can be programmed to access the edge selection circuitry (Figure 3).

The input trip point for detecting a high or low input level is set at $V_{CC} \div 2$.

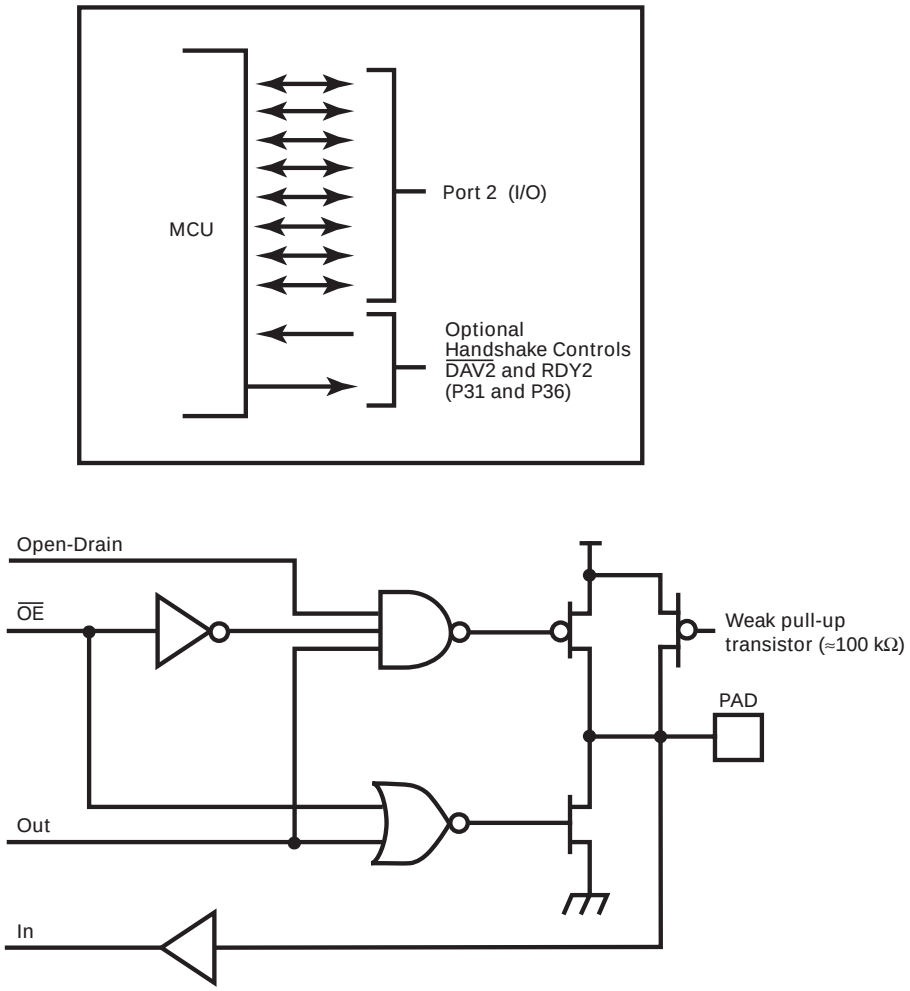


Figure 3. Port 2 Configuration

Port 3 (P37–P31). Port 3 is a 7-bit, CMOS compatible port. Port 3 consists of three fixed inputs (P33–P31) and four fixed outputs (P37–P34), and can be configured under software control for Input/Output, Interrupt, Port handshake, Data Memory functions, and output from the counter/timers. P31, P32, and P33 are standard CMOS inputs; outputs are push-pull.

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge-triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge detection circuit is through

P31 or P20 (see CTR1 Register Description). P31 must be in DIGITAL mode to access the Timer Edge Detection circuit. To access Edge Detection with P31 in ANALOG mode, P20 must be selected as the Timer Edge Detection input. If the comparator output of P31 is used as the edge detection input source, then the comparator output must be enabled on P34 (PCON Bit D0 = 0) and P34 must connect to P20. P20 must be configured as the edge detection (demodulator) input.

Note: *The above results in P31 analog comparator output being enabled on P34 if P34 is not selected as a timer output.*

Port 3 provides the following control functions:

1. Handshake for Ports 0, 1, and 2 ($\overline{DAV}$ and RDY).
2. 3 external interrupt 24 signals (IRQ2–IRQ0).
3. Data Memory Select ($\overline{DM}$—see Table 1).

Port 3 also provides output for each of the counter/timers and the AND/OR/NAND/NOR Logic. Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0 and bit 0 of CTR2.

Table 1. Pin Assignments

Pin No	I/O	C/T	Comp.	Interrupt	P0 HS	P1 HS	P2 HS	Ext
Pref1	Input		RF1					
P31	Input	Input	AN1	IRQ2			D/R	
P32	Input		AN2	IRQ0	D/R			
P33	Input		RF2	IRQ1		D/R		
P34	Output	T8	A01			R/D		DM
P35	Output	T16			R/D			
P36	Output	T8/16					R/D	
P37	Output		A02					
P20	I/O	Input						

Notes:
HS = Handshake Signals.
D = $\overline{DAV}$.
R = RDY.

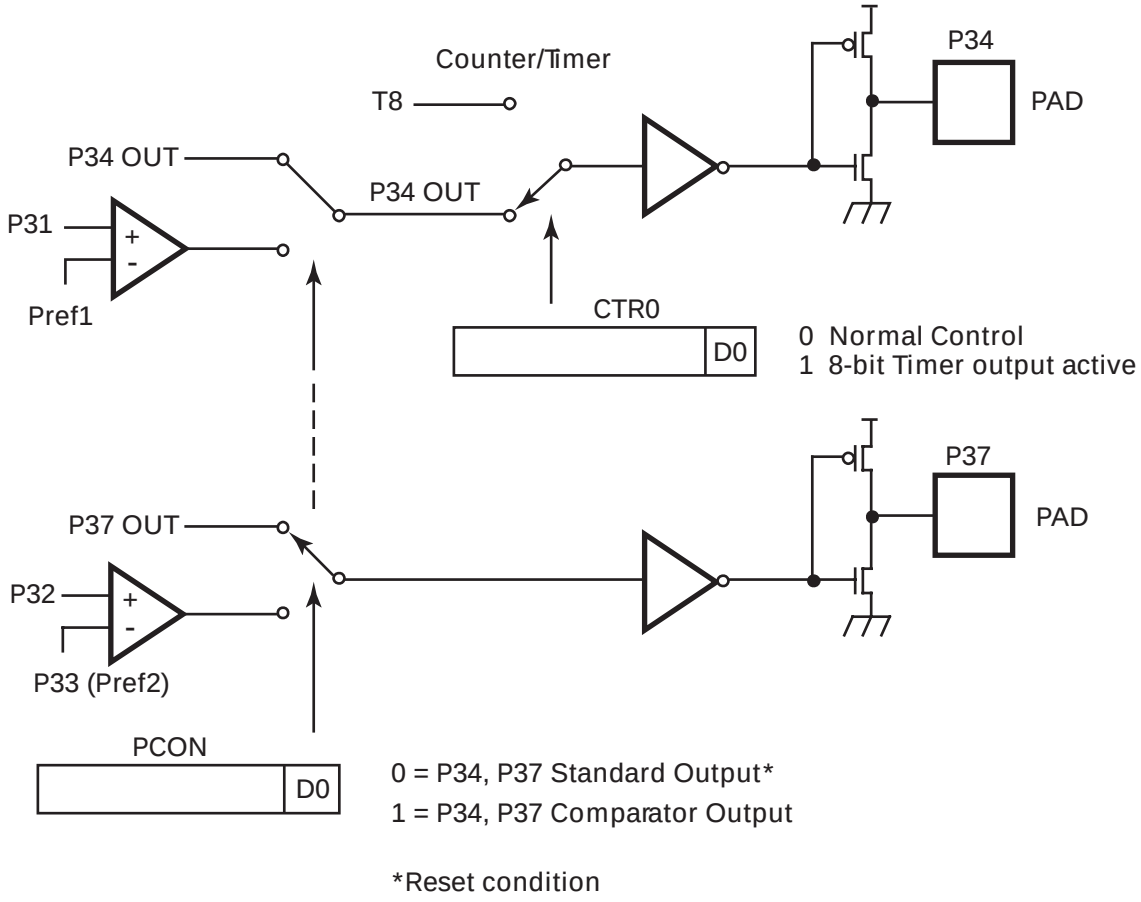


Figure 4. Port 3 Configuration

Comparator Inputs. In Analog mode, Port 3 (P31 and P32) features a comparator front end (Figure 4). The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 is diverted to the SMR Sources (excluding P31, P32, and P33) as displayed in Figure 5. In digital mode, P33 is used as D3 of the Port 3 input register, thereby generating IRQ1 as illustrated in Figure 6.

When P31 is used as a counter timer input for DEMODULATION mode, P31 must be in DIGITAL mode only.

Note: *Comparators are powered down by entering STOP mode. For P31–P33 to be used as a Stop Mode Recovery source, these inputs must be placed into DIGITAL mode.*

Comparator Outputs. These may be programmed to be output on P34 and P37 through the PCON register (Table 26).

$\overline{\text{RESET}}$ (Input, active Low). This pin initializes the MCU. Reset is accomplished either through Power-On, Watchdog Timer, Stop Mode Recovery, Low-Voltage Detection, or external reset. During Power-On, V_{LV}, and Watchdog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions. No pull-up is provided internally. There is no internal condition that does not allow an external reset to occur. There is a ROM Mask Option that disables the internal driving of the reset pin during POR and WDT reset by disabling the pull-down transistor connected to the reset pin.

After the POR time, $\overline{\text{RESET}}$ is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter consisting of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock, after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset (whichever is longer).

During the reset cycle, $\overline{\text{DS}}$ is held active Low while $\overline{\text{AS}}$ cycles at a rate of TpC ÷ 2. Program execution begins at location 000Ch, 5–10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is T_{POR}. The WDTMR, SMR, P2M, P2, P3, or P3M registers do not reset on a Stop Mode Recovery operation.

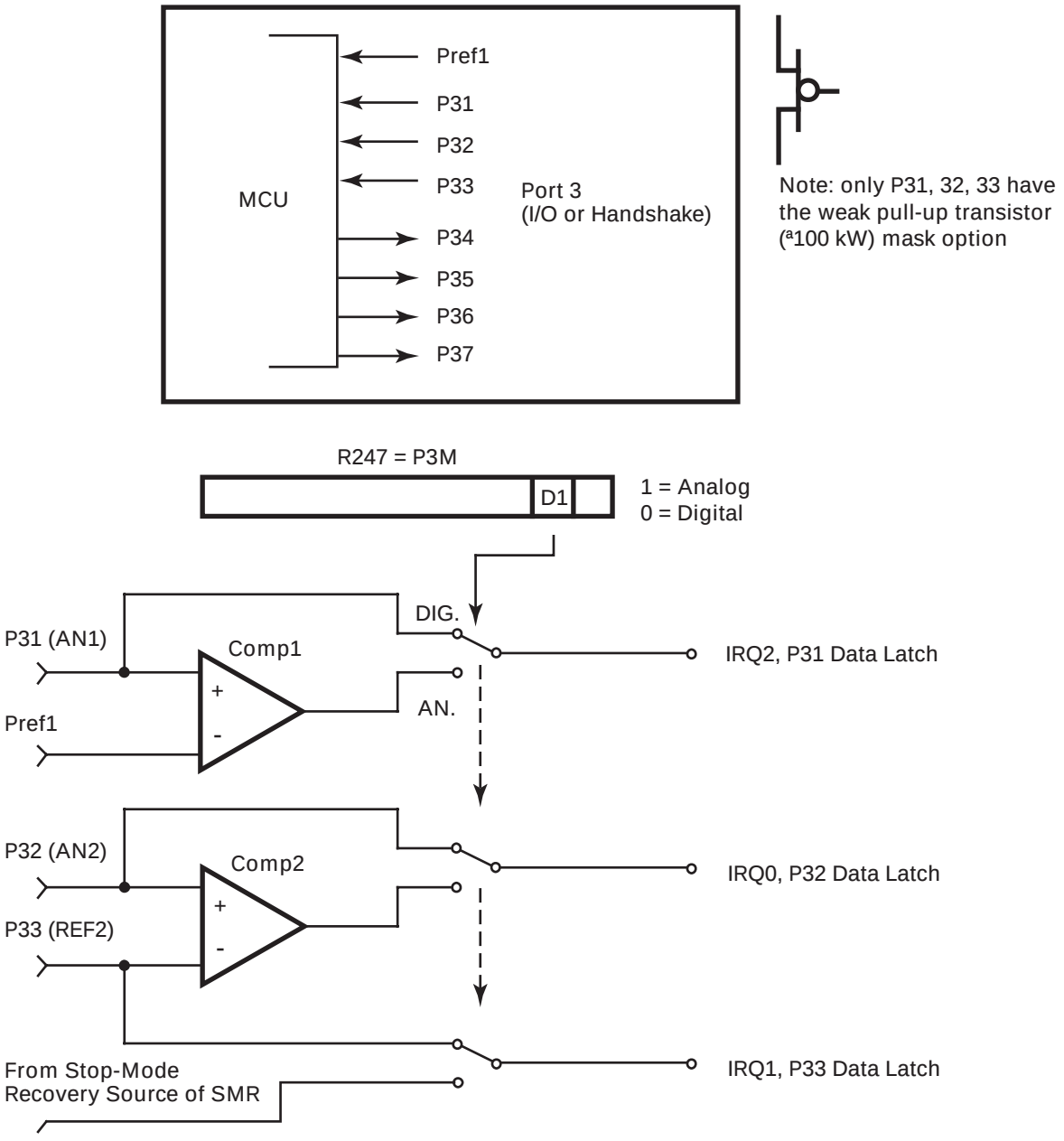


Figure 5. Port 3 Configuration

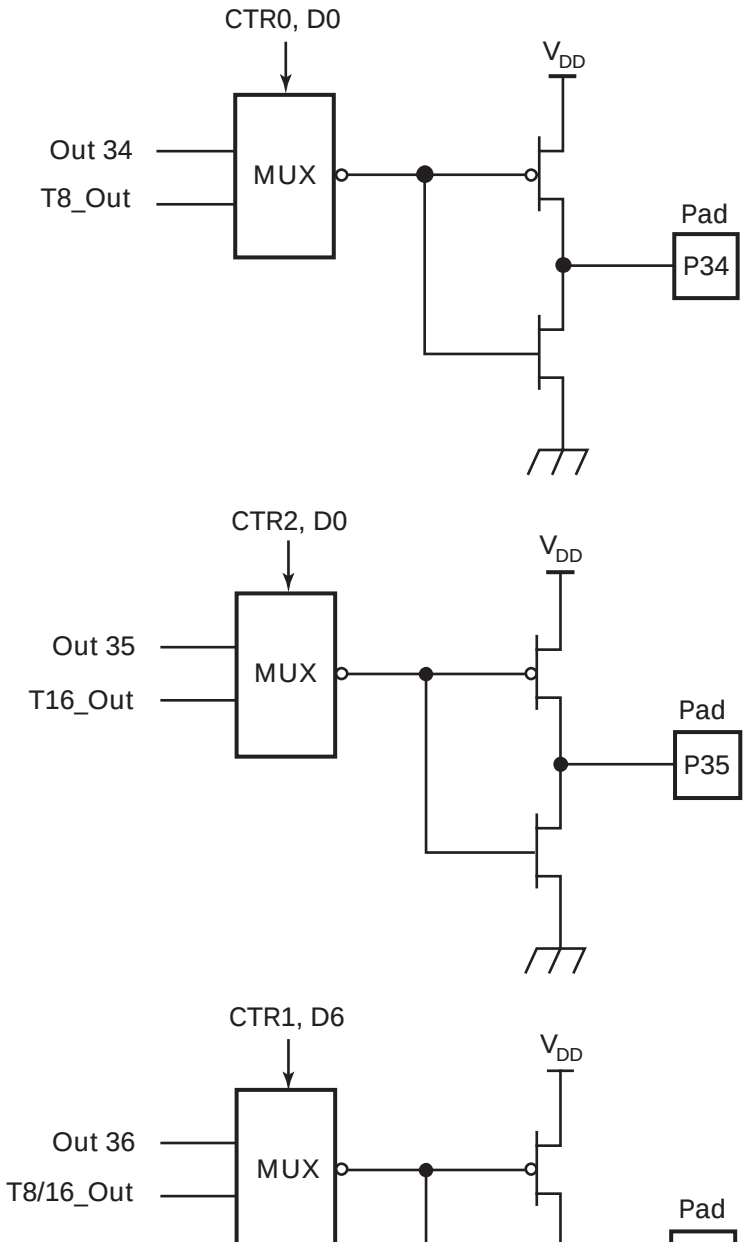


Figure 6. Port 3 Configuration

Functional Description

The Z8 incorporates special functions to enhance functionality in consumer and battery operated applications.

Reset. The Z8 resets when one of the following conditions occurs:

1. Power-On Reset
2. Watchdog Timer
3. Stop Mode Recovery Source
4. Low-Voltage Detection
5. External Reset

Program Memory. The Z8 addresses up to 16K of Internal Program Memory, with the remainder residing in external memory (Figure 1). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain five 16-bit vectors that correspond to the five available interrupts. At addresses 16KB and greater, the Z8 executes external program memory fetches (see Table 2). Port 0 and Port 1 must be configured for external memory access.

RAM. The Z8 features 748 bytes of general-purpose RAM. There are 236 bytes in the Register file. The remaining 512 bytes make up the Extended Data RAM.

Extended Data RAM. The Extended Data RAM occupies the address range FE00h–FFFFh (512 bytes). This range of external addresses is replaced by the internal Extended Data RAM and cannot be used to directly write to or read from External Memory. Accessing the Extended Data RAM is accomplished by using LDE, LDEI, LDC, or LDCI instructions. Port 1 and Port 0 are free to be set as I/O or ADDR/DATA modes (except for high-impedance) when accessing Extended Data RAM. In addition, if the External Memory uses the same address range as the Internal Extended Data RAM, the External Memory can be used as External Stack only.

Notes: *1. The Extended Data RAM cannot be used as STACK or instruction/code memory. Accessing Extended Data RAM dictates the following condition: P01M register bits D4–D3 cannot be set to 11.*

2. The L71 Emulator features 1024 bytes of hardwired Internal Extended Data RAM from FC00h to FFFFh.

3. The L71 Emulator requires Register P01M Bit D4 = 1, D3 = 0 to access Extended Data RAM and configure Emulator Register P1EM (0Ch) Bank D.

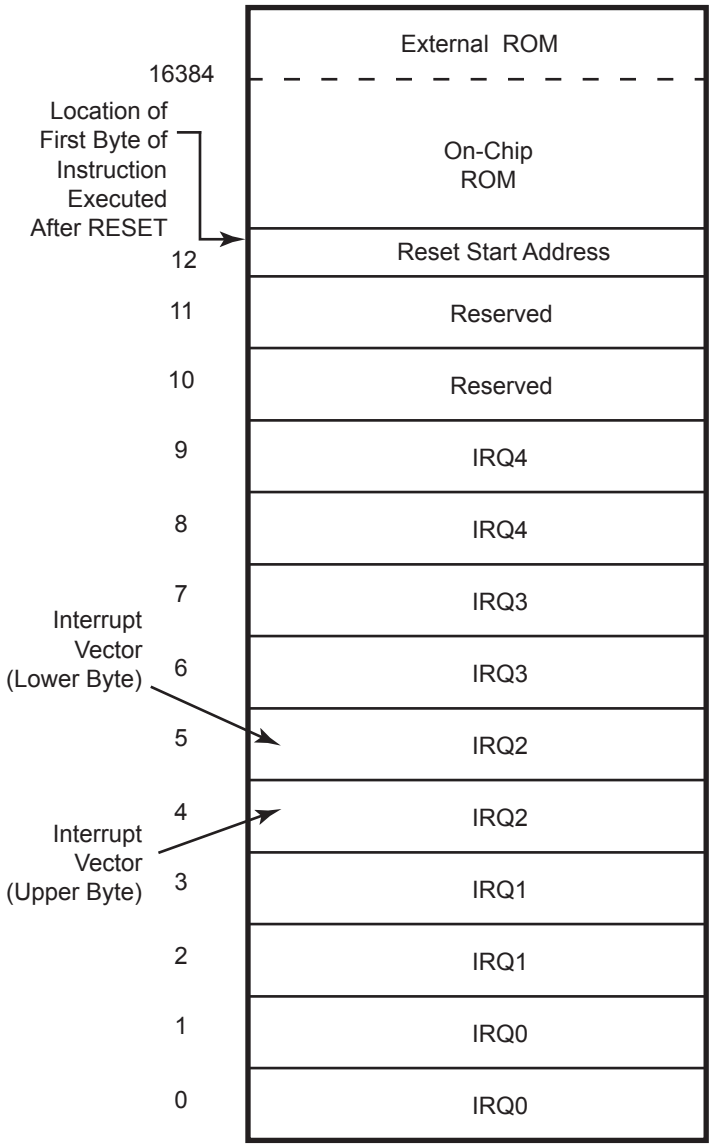


Figure 1.Program Memory Map

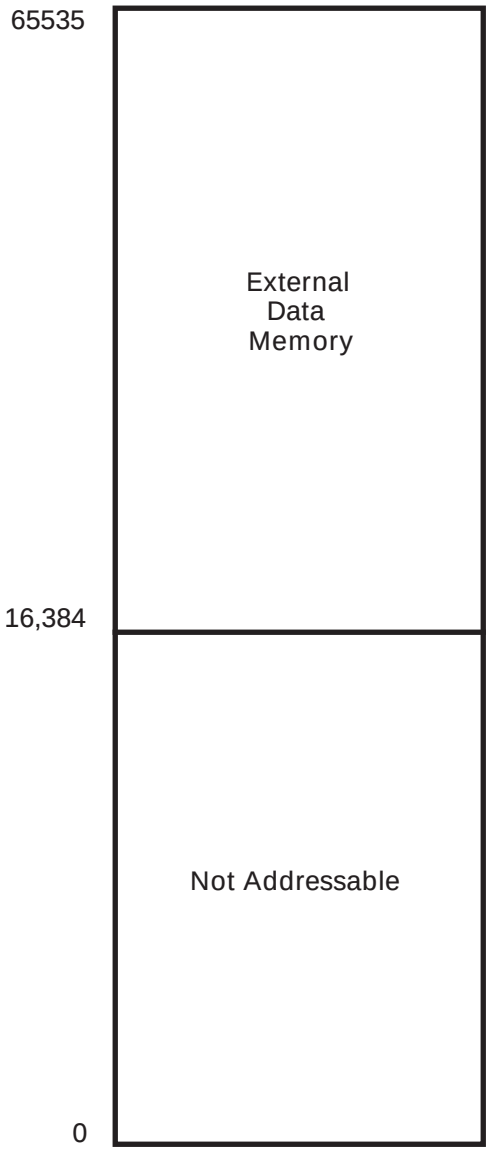


Figure 2.Data Memory Map

External Memory ($\overline{DM}$). The Z8 addresses up to 48K bytes (minus Extended Data RAM space) of external memory beginning at address 16384 (Figure 2). External data memory is included with, or separated from, the external program memory space. $\overline{DM}$, an optional I/O function that is programmed to appear on P34, is used to distinguish between data and

program memory space. The state of the $\overline{DM}$ signal is controlled by the type of instruction being executed. An LDC Op Code references PROGRAM ($\overline{DM}$ inactive) memory, and an LDE instruction references data ($\overline{DM}$ active Low) memory.

Expanded Register File. The register file is expanded to allow for additional system control registers, and for mapping of additional peripheral devices into the register address area. The Z8 register address space R0 through R15 is implemented as 16 banks of 16 registers per bank. These register banks are known as the ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

The upper nibble of the register pointer (Figure 3) selects which working register group of 16 bytes are accessed out of the possible 256 in the register file. The lower nibble selects the expanded register file bank and, in the case of the Z86C72 family, banks 0, F, and D are implemented. A `0h` in the lower nibble allows the normal register file (bank 0) to be addressed, but any other value from 1H to `Fh` exchanges the lower 16 registers to an expanded register bank (see Figure 3).

Example:

R253 RP = 00h
R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0Dh
R0 = CTRL0
R1 = CTRL1
R2 = CTRL2
R3 = Reserved

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

LDRP, #0DhSelect ERF D for access to bank D (working register group 0)

LDR0,#xxLoad CTRL0

LDR1, #xxLoad CTRL1

LDR1, 2CTRL2 → CTRL1

LDRP, #7DhSelect expanded register bank D and working register group 7 of bank 0 for access.

LD71h, R2CTRL2 → register 71h

LDR1, R2CTRL2 → register 71h

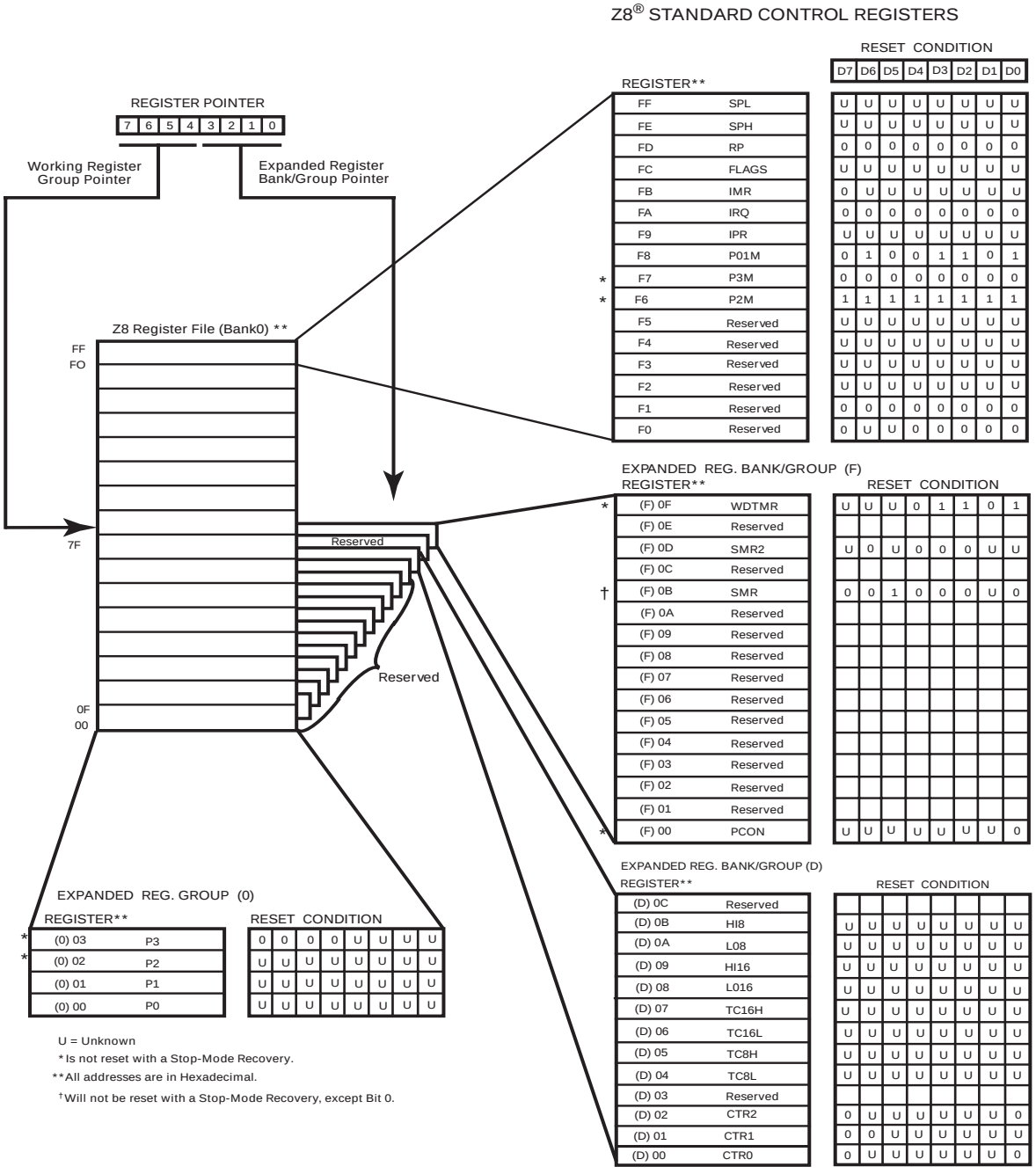


Figure 3.Expanded Register File Architecture

Register File. The register file (bank 0) consists of four I/O port registers, 236 general-purpose registers, and 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively). In addition, two expanded register groups (Banks D and F) are also included. Instructions can access registers directly or indirectly through an 8-bit address field. This option allows a short, 4-bit register address using the Register Pointer (Figure 4). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: *The working register group E0–EF can only be accessed through working registers and indirect addressing modes.*

Stack. The external data memory or the internal register file is used for the stack. An 8-bit Stack Pointer (Table 15) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Note: *When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH are loaded into Port 0 whenever the internal stack is accessed.*

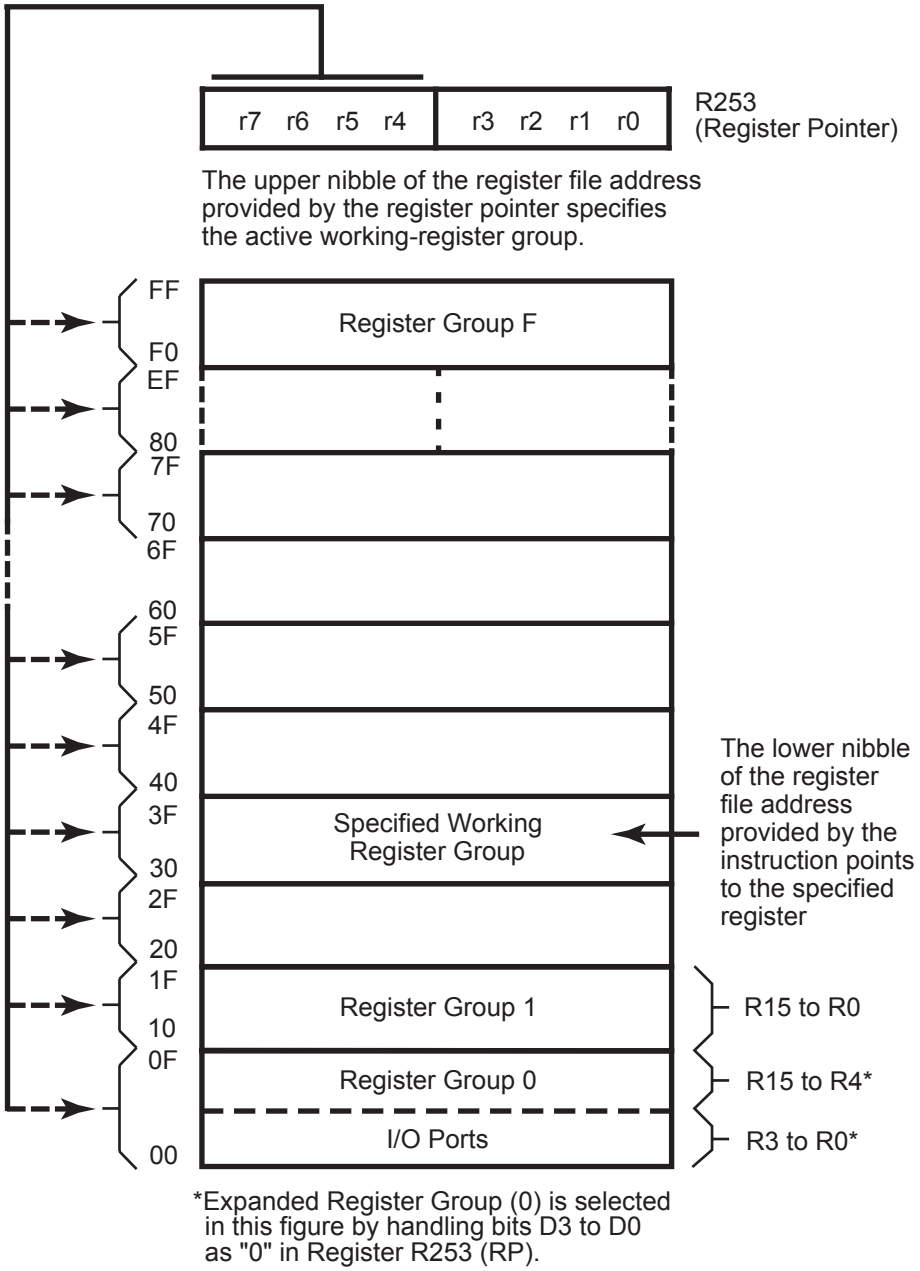


Figure 4. Register Pointer—Detail

Interrupts: The Z8 features five different interrupts. The interrupts are maskable and prioritized (Figure 5). The five sources are divided as follows: three sources are claimed by Port 3 (lines P33–P31), while the remaining two are held by the counter/timers (Table 1). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

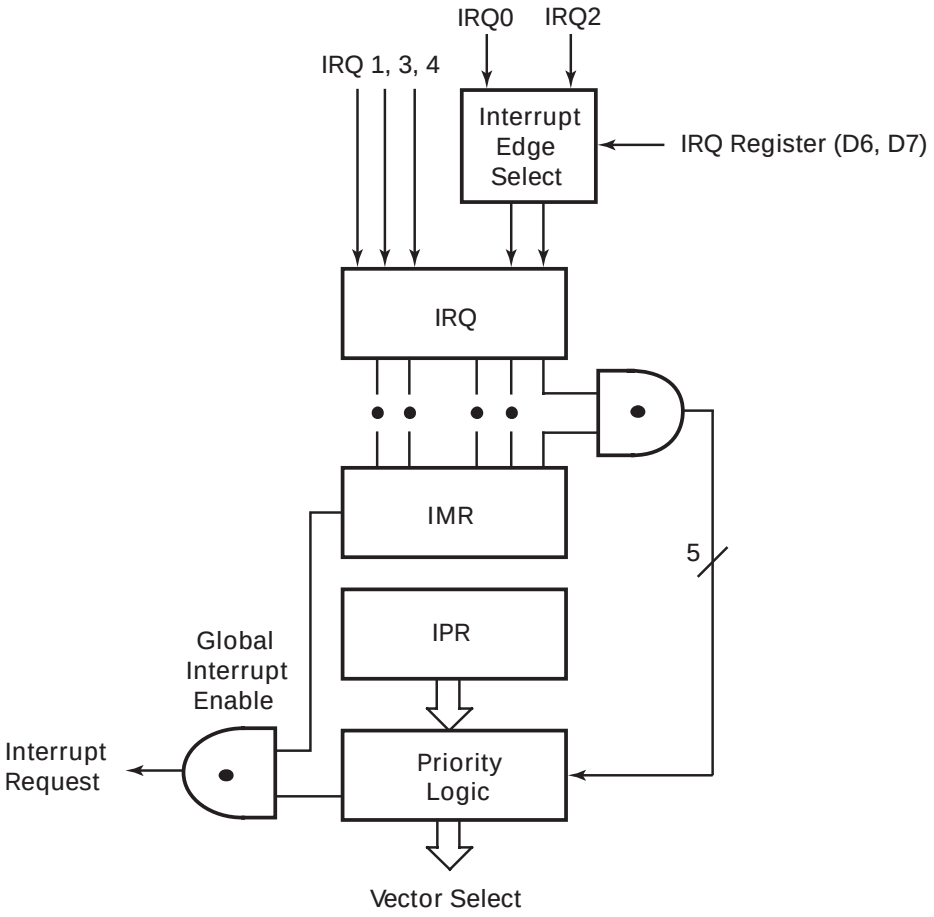


Figure 5. Interrupt Block Diagram

Table 1. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	$\overline{DAV0}$, IRQ0	0,1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2,3	External (P33), Falling Edge Triggered
IRQ2	$\overline{DAV2}$, IRQ2, T_{IN}	4,5	External (P31), Rising/Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle is activated when an interrupt request is granted. This cycle disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge-triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (see Table 2), bits D7 and D6. The Interrupt Edge Select configuration is shown in Table 1.

Clock. The on-chip oscillator features a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (X_{IN} = Input, X_{OUT} = Output). The crystal should be AT-cut, 1 MHz to 16 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z8 on-chip oscillator may be driven with a cost-effective RC network or other suitable external clock source.

Table 2. IRQ Register

IRQ		Interrupt Edge	
D7	D6	IRQ2 (P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F

Table 2. IRQ Register

IRQ		Interrupt Edge	
D7	**D6**	**IRQ2 (P31)**	**IRQ0 (P32)**
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge
In ANALOG mode, the Stop Mode Recovery sources selected by the SMR register are connected to the IRQ1 input. Any of the Stop Mode Recovery sources for SMR (except P31, P32, and P33) can be used to generate IRQ1 (falling edge triggered).

The crystal should be connected across X_{IN} and X_{OUT} using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from X_{IN} to X_{OUT}, with a frequency-setting capacitor from X_{IN} to Ground (Figure 6).

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power Fail to Power OK status.
2. Stop Mode Recovery (if D5 of SMR = 1).
3. WDT Time-Out.

The POR time is T_{POR}. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop Mode Recovery (typical for external clock, RC, or LC oscillators).

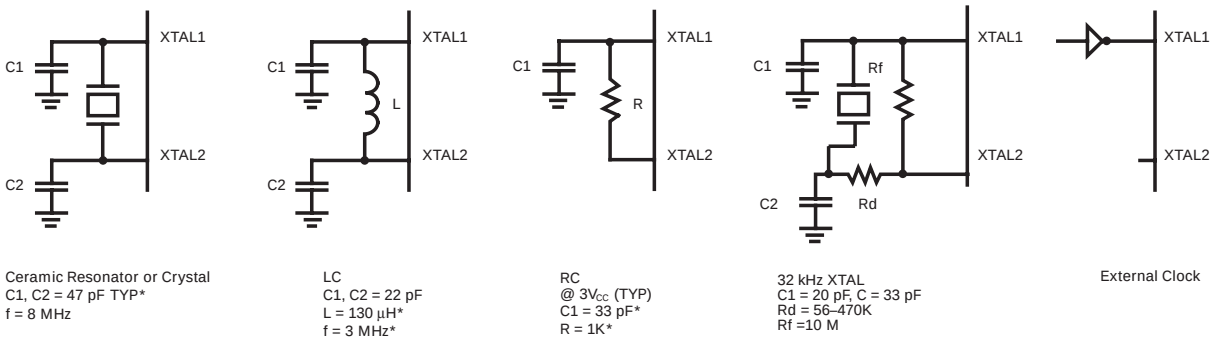


Figure 6. Oscillator Configuration

HALT. HALT turns off the internal CPU clock, but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. The STOP instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. STOP mode is terminated only by a reset, such as WDT time-out, POR, SMR, or external reset. This condition causes the processor to restart the application program at address `000Ch`. To enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Op Code = `FFh`) immediately before the appropriate sleep instruction. For example:

```
FFNOP; clear the pipeline
6FSTOP; enter STOP mode
```

or

```
FFNOP; clear the pipeline
7FHALT; enter HALT mode
```

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2, and 3, and low-EMI oscillator. The PCON register is located in the expanded register file at Bank F, location `00h` (Table 3).

Table 3. Port Configuration Register—PCON 00h/R0 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7	Oscillator	W	1	**Low-EMI Oscillator** 0: Low EMI 1: Standard
D6	Port 3 I/O	W	1	**Port 3** 0: Low EMI 1: Standard
D5	Port 2 I/O	W	1	**Port 2** 0: Low EMI 1: Standard
D4	Port 1 I/O	W	1	**Port 1** 0: Low EMI 1: Standard
D3	Port 0 I/O	W	1	**Port 0*** 0: Low EMI 1: Standard
D2	Port 0 I/O	W	1	**Port 0** 0: Open-Drain 1: Push-Pull Active
D1	Port 1 I/O	W	1	**Port 1*** 0: Open-Drain 1: Push-Pull Active
D0	Port 3	W	0	**Port 3 Comparator Output** 0: P34, P37 Standard Output 1: P34, P37 Comparator Output
Note: Must be set to 1 for devices in 28-pin packages.				

Comparator Output Port 3 (D0). Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Stop Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop Mode Recovery (Table 4). All bits are WRITE ONLY except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop Mode Recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recov-

ery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bit D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0Bh.

Table 4. Stop Mode Recovery Register 1—SMR1 0Bh/R11 Bank Fh: WRITE ONLY, except Bit D7, which is READ ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	W	W	W	W	W	W	W
Reset	0	0	1	0	0	0	0	0
Note: R = Read, W = Write, X = Indeterminate.								

Bit Position	Bit Field	R/W	State	Description
D7	STP	R	0	**Stop Flag** 0: POR 1: Stop Mode Recovery
D6	SMR	W	0	**Stop Mode Recovery Level** 0: Low 1: High
D5	STPDLY	W	1	**Stop Delay** 0: Off 1: On
D4–D2	SMRSRC	W	000	**Stop Mode Recovery Source2** 000: POR only and/or external RESET 001: P30 010: P31 011: P32 100: P33 101: P27 110: P2 NOR 0–3 111: P2 NOR 0–7
D1	EXTCLK	W	0	**External Clock Divide-by-2** 0: SCLK ÷ TCLK = Crystal ÷ 2 1: SCLK = Crystal
D0	CLK	W	0	**SCLK ÷ TCLK Divide-by-16** 0: Off[1] 1: On

Notes:
1. Do not use in conjunction with SMR2 Source.
2. Cleared by RESET and SMR.

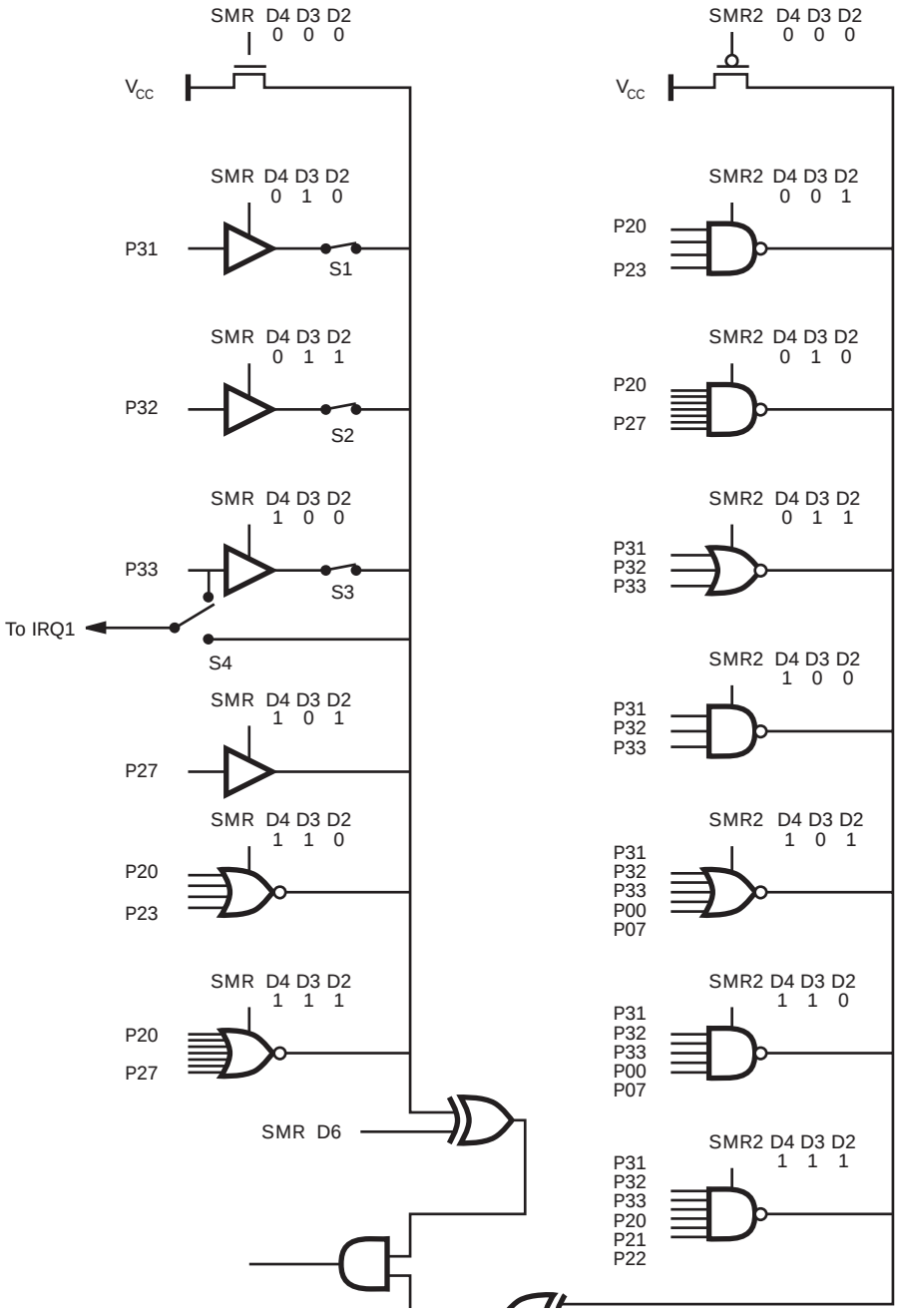


Figure 7. Stop Mode Recovery Source

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

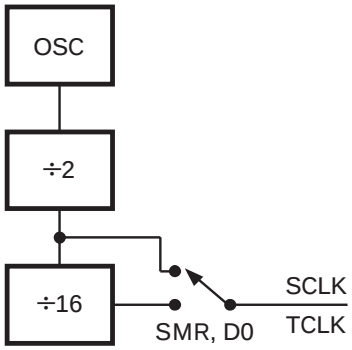


Figure 8. SCLK Circuit

Stop Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake up source of the Stop Mode Recovery (Figure 7 and Table 5).

Table 5. Stop Mode Recovery Source

D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

P33–P31 cannot wake up from STOP mode if the input lines are configured as analog input.

Note: *For NAND Stop Mode Recovery, any Port 2 bit defined as an output drives the corresponding input to the default state. This definition allows the remaining inputs to control the NAND function. Refer to the SMR2 Register on the next page.*

Stop Mode Recovery Delay Select (D5). This bit, if Low, disables the 5 ms $\overline{\text{RESET}}$ delay after Stop Mode Recovery. The default configuration of this bit is 1. If the *fast* wake-up is selected, the Stop Mode Recovery source must be kept active for at least 5TpC.

Stop Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z8 from STOP mode. A 0 indicates low-level recovery. The default is 0 on POR (Figure 9).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode, and is a Read Only Flag bit. A 1 in D7 (warm) indicates that the device wakes up from a SMR source or a WDT while in STOP mode. A 0 in this bit (cold) indicates that the device is reset by a POR, WDT while not in STOP mode, or the device was awakened by a low-voltage STANDBY mode.

Stop Mode Recovery Register 2 (SMR2). This register contains additional Stop Mode Recovery sources. When the Stop Mode Recovery sources are selected in this register then SMR register bits D2, D3, and D4 must be 0.

Note: *Port pins configured as outputs are ignored as a NAND SMR2 recovery source. For example, if the NAND of P23–P20 is selected as the recovery source and P20 is configured as an output, then the remaining SMR pins (P23–P21) form the NAND equation.*

Table 6. Stop Mode Recovery Register 2—SMR2 0Dh/R13 Bank Fh: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	X	X	X	0	0

Note: R = Read, W = Write, X = Indeterminate.

Bit/ Field	Bit Position	R/W	State	Description
D7–D2	Reserved	W	X	Reserved—must be 0
D1–D0	STOP Mode	W	00	**Stop Mode Recovery Source 2*** 00: POR only 01: AND P20, P21, P22, P23 10: AND P20, P21, P22, P23, P24, P25, P26, P27

Note: *Do not use in conjunction with SMR Source.

Watchdog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the X_{IN} pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with Bit 4 of the WDT register. Bits 0 and 1control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Table 7). This register is accessible only during the first 60 processor cycles (120 crystal clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop Mode Recovery (Figure 7). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0Fh.

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within the first 64 internal system clocks. After that, the WDTMR is WRITE-protected.

Note: *WDT time-out while in STOP mode does not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 & 3 Data Registers, but the POR delay counter is still enabled even though the SMR stop delay is disabled.*

Table 7. Watchdog Timer Mode Register—WDTMR 0Fh/R15: WRITE ONLY

Bit	D7	D6	D5	D4	D3	D2	D1	D0
R/W	W	W	W	W	W	W	W	W
Reset	X	X	X	0	1	1	0	1

Note: R = Read, W = Write, X = Indeterminate.

Bit/ Field	Bit Position	R/W	State	Description
D7–D5	Reserved	W	X	Reserved—must be 0
D4	X_{IN}	W	0	**XIN/INT RC Select for WDT** 0: On-Board RC 1: Crystal
D3	WDT	W	1	WDT During STOP
D2	WDT	W	1	WDT During HALT

Note: Not used in conjunction with SMR Source.

D1–D0	WDT Tap	W	01	**WDT Tap**	**Int RC OSC**	**System Clock**
				00:	3.5 ms	128 SCLK
				01:	10.0 ms	256 SCLK
				10:	14.0 ms	512 SCLK
				11:	56.0 ms	2048 SCLK

Note: Not used in conjunction with SMR Source.

WDT Time Select (D0, D1). These bits select the WDT time period. It is configured as shown in Table 8.

Table 8. WDT Time Select

D1	D0	Time-Out of Internal RC OSC	Time-Out of Crystal Clock
0	0	2 ms min	256 TpC
0	1	4 ms min	512 TpC
1	0	8 ms min	1024 TpC
1	1	32 ms min	4096 TpC

Note: TpC = crystal clock cycle. The default on reset is 2 ms.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Because the crystal clock is stopped during STOP mode, the on-board RC must be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, X_{IN}. The default configuration of this bit is 0, which selects the RC oscillator.

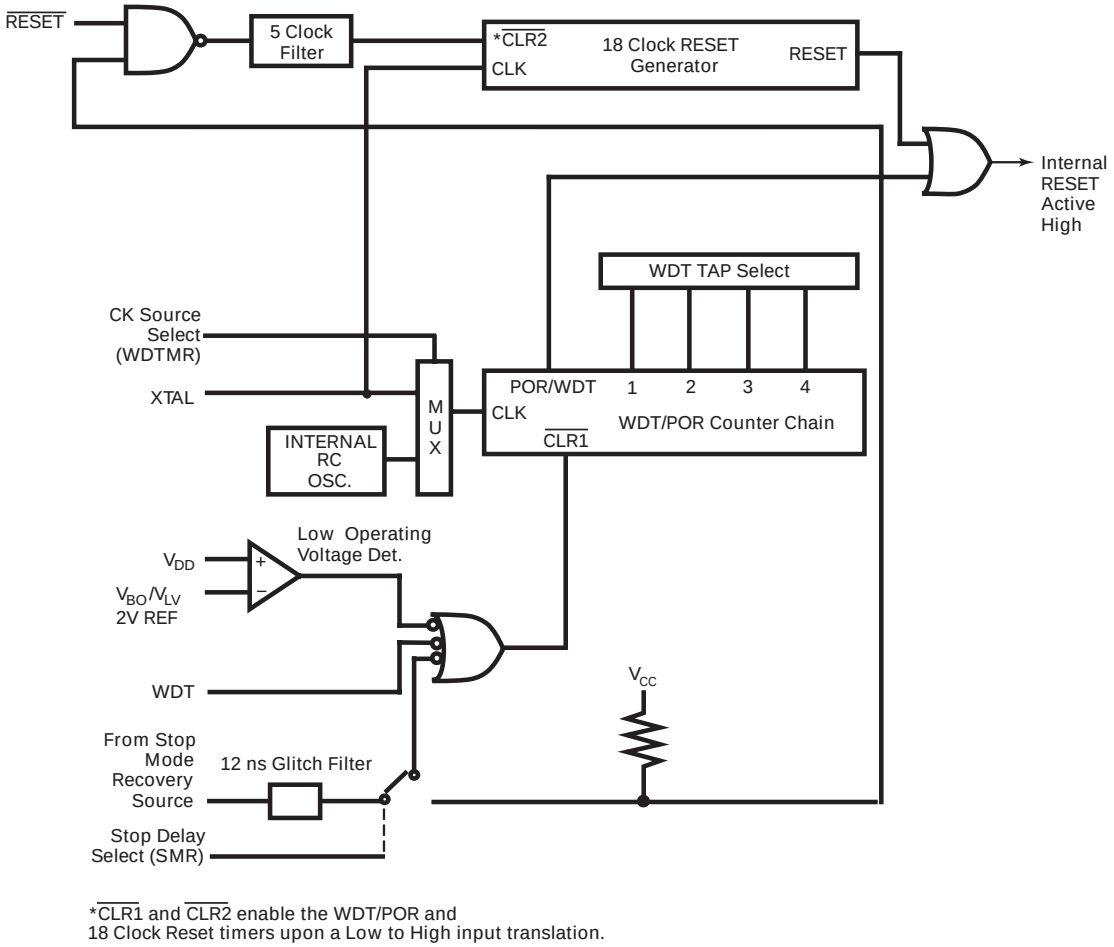


Figure 9. Resets and WDT

Mask Selectable Options. There are seven Mask Selectable Options to choose from based on ROM code requirements. (See Table 9).

Table 9. Mask Selectable Options

Option	Function
RC/Other	RC/CRYSTAL
32 kHz crystal	On/Off
Port 04–07 weak pull-up transistor	On/Off

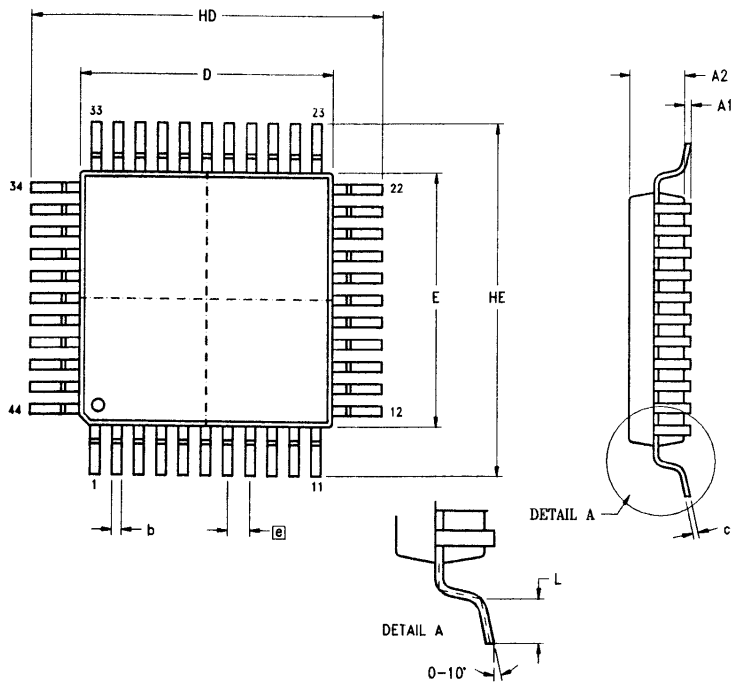
Table 9. Mask Selectable Options

Option	Function
Port 00–03 weak pull-up transistor	On/Off
Port 31–33 weak pull-up transistor	On/Off
Port 20–27 weak pull-up transistor	On/Off
Pull-Down Transistor On Reset Pin	On/Off

Low-Voltage Detection/Standby. An on-chip Voltage Comparator checks that the V_{CC} is at the required level for correct operation of the device. Reset is globally driven when V_{CC} falls below V_{LV}. A small further drop in V_{CC} causes the X_{IN} and X_{OUT} circuitry to stop the crystal or resonator clock. Typical Low-Voltage power consumption in this LOW VOLTAGE STANDBY mode (I_{LV}) is about 45 µA (varying with the number of Mask selectable options enabled). If the V_{CC} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{LV}, the device performs a POR and function normally (Figure 9).

The minimum operating voltage varies with the temperature and operating frequency, while V_{LV} varies with temperature only.

Package Information



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 1. 44-Pin LQFP Package Diagram

Ordering Information

Z86C72 Available Packages	
Standard Temperature	
44-pin LQFP	Z86C7216FSC

For faster results, contact your local Zilog sales offices for assistance in ordering the part(s) required.

Code Example	
Preferred Package	F = Plastic Dual In-Line Package
Speed	16 = 16 MHz
Standard Temperature	S = 0°C to +70°C
	E = –40°C to +70°C
Environmental Flow	C = Plastic Standard

Part Number Description

Zilog part numbers consist of a number of components. For example, part number Z86C7216FSC is a Z86C72 DIP that operates in the 0ºC to +70ºC temperature range, with Plastic Standard Flow. The Z86C7216FSC part number corresponds to the code segments indicated in the following table.

Z	Zilog Prefix
86	Z8 MCU
C72	Product Number
16	Speed
F	Package
E	Temperature
C	Environmental Flow

Index

R

S

T

W

X

Z

Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.