IMPROVING MEMORY ACCESS TIMING IN Z182 APPLICATIONS

By using the Z182 Microprocessor to improve memory access timing, designers can reduce overall system cost and improve system performance.

1.0 INTRODUCTION

Memory speed requirements have become a major concern in applications such as V.FAST modem control, where processor operating frequencies approaching 33 MHz are required. This application note will demonstrate the calculations of both ROM and RAM access timing, and provide examples of a conventional processor/memory interface design. An alternate approach to processor/memory design will also be presented. The benefits of the alternate approach include permitting the use of slower and less costly ROMs and RAMs; a lower processor operating frequency without reducing system performance and without significant increase in overall system power consumption.

2.0 CONVENTIONAL DESIGN METHODOLOGY

In a conventional design approach for RAM, the processor /RD and /WR signals drive the corresponding RAM inputs directly. In the case of ROM/OTP, once again /RD and /WR are used directly to control the /RD input, and in FLASH memories /PGM. However, the Z182 processor's /RAMCS signal controls the RAM chip select function, while the /ROMCS signal controls the ROM chip select function. Figures 1 and 2 represent a conventional design approach in the processor interface with both ROM/OTP/FLASH and RAM devices.

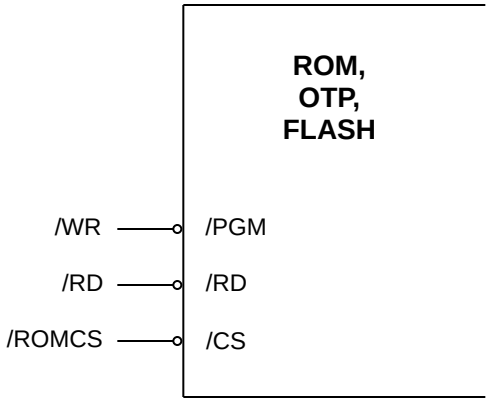

Figure 1. ROM/OTP/FLASH Interface

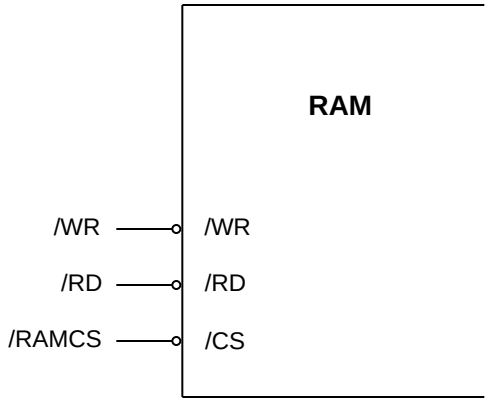

Figure 2. RAM Interface

2.1 Memory Read Access Time

Figures 3 and 4 represent a Z182 machine cycle and depict key timing factors in the overall design consideration for memory read access requirements. There are two separate types of memory reads which need to be addressed. Figure 3 demonstrates an Opcode Fetch cycle. Figure 4 represents all other memory read cycles. The significant difference is that data must be presented by memory to the processor prior to the leading edge of T3 for an Opcode fetch cycle. All other memory read cycles relax the data access requirement in that data is not required by the processor until the trailing edge of T3.

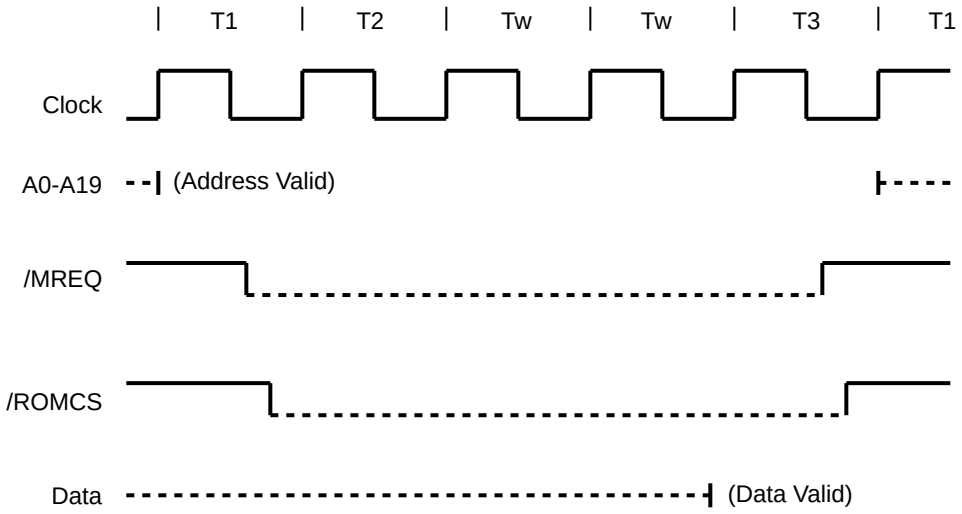

Figure 3. OPCODE Fetch Timing

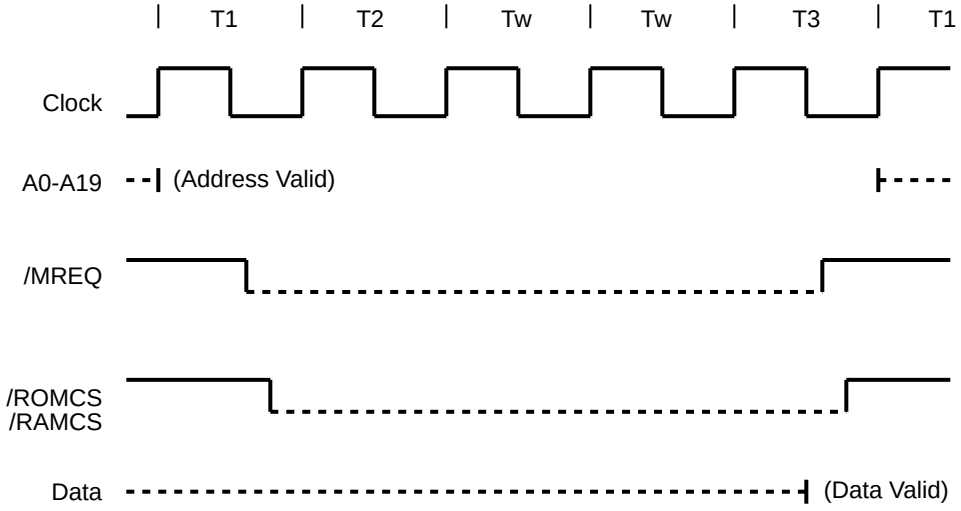

Figure 4. Memory Read Timing

There are several parameters that need to be considered when determining memory read access timing. These parameters are specified in the Z182 Preliminary Product Specification under Z8S180 AC Characteristics. The parameters needed to demonstrate this example are shown in Table 1.

Table 1. Memory Read Access Timing Parameters

Symbol	No.	Parameter
tcy	1	Clock Cycle Time
tad	6	Address Valid from Clock Rise
tMED1	8	Clock Fall to /MREQ Fall Delay
tDRS	15	Data Read Setup Time
TdCS	71	/MREQ Valid to /ROMCS, /RAMCS Valid Delay

2.2 OPCODE Fetch Calculations

A set of equations can be created to determine ROM Opcode Fetch Timing requirements. These equations represent designs with 0 to 3 Wait States:

tacc (0WS) = 1.5(tcy) - T8 - T71 - T15
tacc (1WS) = 2.5(tcy) - T8 - T71 - T15
tacc (2WS) = 3.5(tcy) - T8 - T71 - T15
tacc (3WS) = 4.5(tcy) - T8 - T71 - T15

This set of equations uses the trailing edge of T1 as the initial memory access cycle starting point, and the rising edge of T3 as the time in the memory cycle at which the processor requires data to be valid. This interval is the maximum possible memory access delay and is a multiple of clock cycles, depending on the number of wait states included in the design. Also, the designer needs to consider any possible clock deviation from a 50% duty cycle. Because a memory opcode fetch is based on different edges of the clock, this duty cycle skew must also be subtracted from the results of the above equations.

2.3 Memory Access Cycles

A more relaxed access time requirement exists for all Memory Read cycles other than that for Opcode Fetch. Once again the trailing edge of T1 is used as the reference point for a memory read cycle. Data is not required to be valid at the processor until the trailing edge of T3. With this data, a new set of equations can be created. These equations will typically serve in calculating RAM Read Access requirements, except for designs which execute code from RAM. In that event, the Opcode Fetch equations need to be used for both ROM and RAM access time calculations. The new equations are as follows:

tacc(0WS) = 2(tcy) - T8 - T71 - T15
tacc(1WS) = 3(tcy) - T8 - T71 - T15
tacc(2WS) = 4(tcy) - T8 - T71 - T15
tacc(3WS0 = 5(tcy) - T8 - T71 - T15

It is not necessary to subtract an additional amount of any clock deviation from a 50% duty cycle as in an Opcode Fetch Cycle because the above equations are based on a time period relative to the trailing edges of both T1 and T3.

2.3.1 Calculation Examples

Examples of calculations of read access time requirements for both ROM and RAM are listed below. These calculations are made at 29.5 MHz clock frequency, and are based on T8 = 10 ns, T71 = 10 ns, and T15 = 15, and are "worse case" numbers for each parameter as shown in the Z182 Preliminary Product Specification.

ROM tacc(0 WS) = 1.5 (33.9 ns) - 35 ns = 15.8 ns
ROM tacc(1 WS) = 2.5 (33.9 ns) - 35 ns = 49.7 ns
ROM tacc(2 WS) = 3.5 (33.9 ns) - 35 ns = 83.6 ns
ROM tacc(3 WS) = 4.5 (33.9 ns) - 35 ns = 117.5 ns
RAM tacc(0 WS) = 2.0 (33.9 ns) - 35 ns = 32.8 ns
RAM tacc(1 WS) = 3.0 (33.9 ns) - 35 ns = 66.7 ns
RAM tacc(2 WS) = 4.0 (33.9 ns) - 35 ns = 100.6 ns

Using the above calculations, the user can select a design which operates at 29.5 MHz and uses 70 ns ROM/OTP/FLASH at 2 Wait States and 25 ns RAM with 0 Wait States.

3.0 IMPROVING MEMORY READ ACCESS TIME

ROM/OTP and FLASH memory are typically controlled in the presentation of data by three parameters:

a. Chip select must be valid for a period of time, equal to the device access prior to data being valid ($Tacc_1$).

b. Likewise, the address lines must also be active for a similar period of time prior to data becoming valid.

c. The output enable must be guaranteed active for a period of time prior to data becoming valid (Figure 5). This duration is considerably less than the device access time (approximately 30 ns for 70 ns devices, 35 ns for 90 ns devices, and 50 ns for 120 ns devices). This parameter becomes the focus for reducing memory access time requirements ($Tacc_2$).

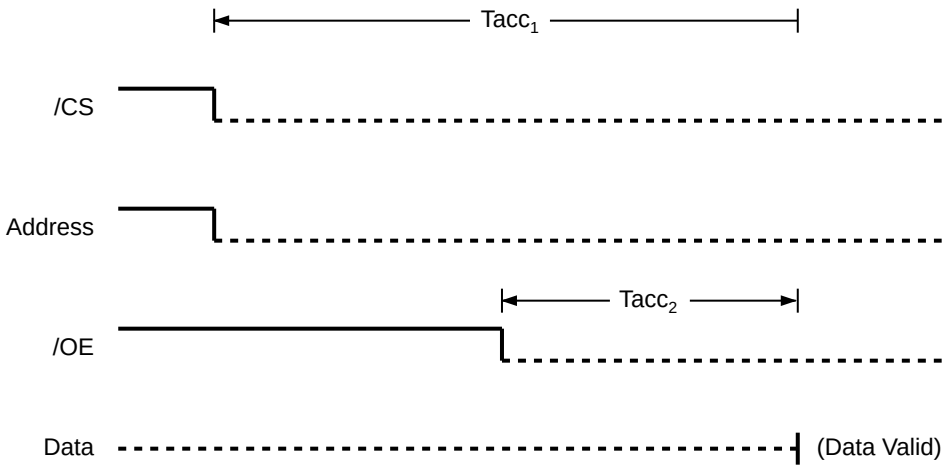

Figure 5. ROM/OTP/FLASH Timing

3.1 ROM Interface Redesign

Consider a variation to the processor/ROM interface shown in Figure 6. In Figure 6, the chip select input is connected to ground, eliminating the memory requirement of access time being dependent on chip select. Figure 6 also shows modifications to both the /PGM and /RD inputs. Two additional OR gates are required to allow /ROMCS to gate both /RD and /WR to the ROM device. This modification relaxes Read Access requirements which are now based on the activation of the /RD input to ROM. Instead of choosing ROMs based on Chip Select or Address Access times, a much faster output enable access time can be used. As mentioned earlier, this requirement is typically 30 ns for 70 ns ROMs, 35 ns for 90 ns ROMs and 50 ns for 120 ns ROMs. The same set of access time equations apply. Therefore, at 29.5 MHz, 2 wait states, the equation yields 83.6 ns, minus the OR gate delay. This satisfies the output enable to data valid requirement of a 70 ns ROM device. The “new” access time requirement permits the use of a slower ROM for 70 ns, as well as 90 ns devices, and possible even 120 ns devices. With 90 ns ROMs, considerable margin exists for additional system design advantages which are covered in the following sections.

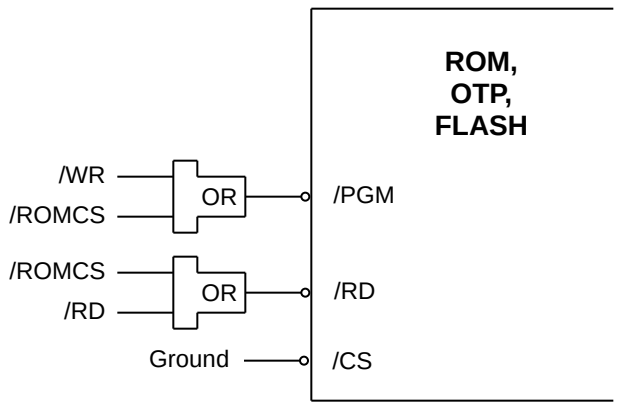

Figure 6. ROM Interface Redesign

3.2 Reducing ROM Wait States

The example used in this application note assumes an initial design based on a 29.5 MHz processor clock, 70 ns ROM/OTP/FLASH with 2 wait states and 25 ns RAM at 0 wait states. A rather simple design change to the processor/ROM interface relaxed ROM access requirements to the point where it becomes possible to use slower, less costly 90 ns ROMs and reducing the ROM wait states from 2 to 1. This, if feasible to the user, will increase overall system performance by as much as 25% in ROM machine cycles. The disadvantages of this approach include the addition of two OR gates plus increased operating power consumption which can be offset by methods which are addressed later in this article.

The read access requirement for an operating frequency of 29.5 MHz, 1 wait state ROM becomes:

ROM tacc(1WS) = 2.5 (33.9 ns)
- 35 ns - OR gate delay
= 49.7 ns - OR gate delay

3.3 Reducing Processor Operating Frequency

It has been demonstrated that the design now permits the use of 90 ns ROMs at 1 wait state, maintaining 25 ns RAMs at 0 wait state, and an operating frequency of 29.5 MHz, the next consideration for reducing overall system cost is to reduce the processor operating frequency. Because a significant increase in processor performance (approximately 20% overall) was achieved by reducing the number of ROM wait states from 2 to 1, this allows a reduction of processor operating frequency by a similar percentage.

Note: The actual performance difference should be measured on an individual basis by making actual measurements on performance-critical code. Assuming a lower processor operating frequency of 25 MHz, the following calculations for both ROM and RAM can be performed:

ROM tacc(1 WS) = 2.5 (40 ns)
- 35 ns - OR gate delay
= 65 ns - OR gate delay

RAM tacc(0 WS) = 2 (40 ns)
- 35 ns = 45 ns

Significant access requirements have been relaxed due to the longer clock cycle. These new calculations suggest even additional system cost reduction since 35 ns RAMs can now be substituted for the original 25 ns devices. Additionally, the design is approaching the possibility of reducing ROM access requirements to 120 ns. Although this is not possible at 25 MHz, due to the need to have the address lines valid a period of time prior to data becoming valid, an additional reduction in processor frequency, if possible in the application, could satisfy 120 ns ROM requirements.

3.4 Improving System Power Consumption

As noted earlier, the suggested modification which connects ROM chip select to ground requires an additional system power consumption of 30 ma, worse case. This increase in power consumption can be offset by operating the processor at a lower frequency. For example, the Z182 worse case current requirement is approximately 6 ma/MHz over operating frequencies from 20 MHz to 33 MHz. The design consideration which led to reducing processor operating frequency from 29.5 MHz to 25 MHz offsets the additional current consumed by ROM as a result of connecting chip select to ground.

4.0 MEMORY INTERFACE DESIGN VERIFICATION

The memory interface design was verified using Zilog's Z8018200ZCO Evaluation Board. Using a TMS 27C512 EPROM with an access time of 150 ns, a firmware test was implemented at 4.5 Volts with 0 Wait State operation. When the frequency was increased to 12.3 MHz, the Z182 failed to execute code from the EPROM when set at 0 Wait State operation, however, the Z8018200ZCO Evaluation Board was reworked to include the memory workaround which resulted in the EPROM test showing significant improvement with continued EPROM operation beyond 20 MHz (Figure 7).

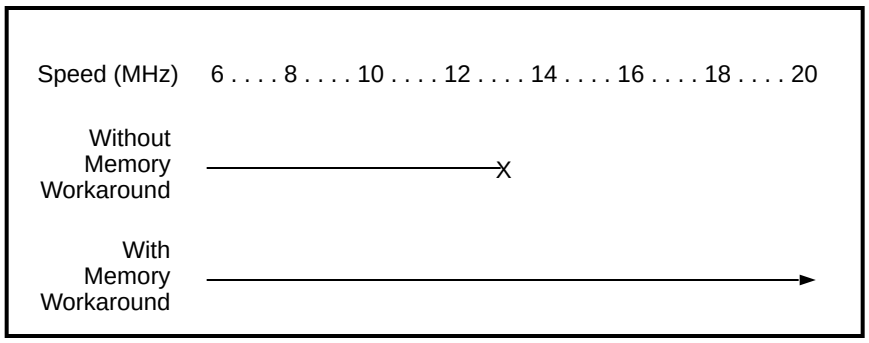

Figure 7. 150 ns EPROM Functional Graph

5.0 ADDITIONAL SUGGESTIONS

By optimizing firmware, code can be manipulated to run more efficiently. Code efficiency can be improved to reduce overall system speed, while maintaining system performance and reduced system speed (not to mention lower noise) directly relates to reduced system cost by allowing slower ROMs. Below are some code optimization techniques:

1. Optimize code fragments commonly used within the system (i.e., interrupt service routines, compression code). These fragments can be programmed in Assembler for speed.
2. Because the Z80182 has an individual Wait State Generator for RAM and ROM, firmware benefits from 0 wait state RAM while allowing for slower ROM accesses. Time critical functions can be loaded into 0 wait state RAM and executed from the RAM area.
3. Make use of the Z182 performance features, such as ESCC and 16550 MIMIC FIFOs, as well as DMAs. (DMAs transfer data to and from memory without the overhead of opcode fetches and interrupt service routines.)

6.0 CONCLUSION

This application note demonstrated the calculations of both ROM and RAM access timing and provided examples of a conventional processor/memory interface design using a 29.5 MHz operating frequency, 70 ns ROM at 2 wait states, and 25 ns RAM at 0 wait states. An alternate approach to processor/memory design was also presented which required two additional OR gates. The benefits of the alternate approach included permitting the use of slower and less costly ROMs and RAMs; a lower processor operating frequency with equal system performance and without significant increase in overall system power consumption.

Note: While this application note demonstrates ways to reduce system cost by using slower ROMs and RAM, if a system design cannnot benefit from slower memories, reduced power consumption, or reduced processor frequency, then system performance can be improved significantly by designing with faster processors and faster memories.

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