Product Update

**Errata for Z8 Encore! XP®
F3224 Series Devices**

UP014204-0323

F3224 Series MCU all Date Codes

The errata listed in Table 1 are found in F3224 Series devices with all date codes. When reviewing the following errata, Zilog recommends that you download the most recent version of the Z8 Encore! XP F3224 Series Product Specification (PS0381) from the Zilog website.

Table 1. Errata to F3224 Series Devices

No.	Summary	Detailed Description
2	RES_{DCO} can be significantly exceeded at certain DCO control codes when the FLL is enabled.	FLL dithering between two DCO control words is normal behavior; however, at certain DCO control words, when the FLL is enabled, the Resolution of the DCO (RES_{DCO}) is significantly larger than specified resulting in dithering between frequencies that are farther apart than implied by RES_{DCO}. **Suggested Workaround:** 1. When the FLL is enabled, use a FLLNDIVH/L value that results in 12MHz ≤ System Clock frequency ≤ 20MHz. When using this workaround, the problematic DCO control words are avoided.
3	VBO does not occur in Stop Mode	When in Stop Mode, the Voltage Brown-Out (VBO) condition does not propagate and does not cause a System Reset. **Suggested Workaround:** Enable the Low Voltage Detection (LVD) and the LVD interrupt. While in Stop Mode, the LVD interrupt causes Stop-Mode Recovery. Once Stop Mode is exited, the VBO condition propagates and causes a System Reset. The LVD threshold level is user defined using the LVD_TRIM field in the TLVD_VBO register.

F3224 Series MCU Date Code 2017 and later

The errata listed in Table 3 are found in F3224 Series devices with date codes prior to and including 2017. When reviewing the following errata, Zilog recommends that you download the most recent version of the Z8 Encore! XP F3224 Series Product Specification (PS0381) from the Zilog website.

Table 2. Errata to F3224 Series Devices

No.	Summary	Detailed Description
1	MCT not available for the 32-pin package option	The Multi-Channel Timer (MCT) is not available for the 32-pin package option. **Suggested Workarounds:** 1. None.

F3224 Series MCU Date Code 1946 only

The errata listed in Table 3 are found in F3224 Series devices with date code 1946 only. When reviewing the following errata, Zilog recommends that you download the most recent version of the Z8 Encore! XP F3224 Series Product Specification (PS0381) from the Zilog website.

Table 3. Errata to F3224 Series Devices

No.	Summary	Detailed Description
1	The LFXO does not function as a Pclk source	The LFXO does not function as a Pclk source. **Suggested Workarounds:** 1. Select the IPO as Pclk by configuring IPOEN=1 and PCKSEL=00 in the CLKCTL1 Register. 2. Select External Clock2 Drive as Pclk and provide an external clock. This can be accomplished by writing GPIO registers to configure PA2 pin for external clock2 input (CLK2IN) and configuring PCKSEL=10 in the CLKCTL1 Register.
2	IDD higher than specified in all operating modes	IDDA, IDDH, IDDS1, and IDDS2 are approximately 160 uA higher than specified. **Suggested Workarounds:** 1. None.

⚠️ **Warning:** DO NOT USE THIS PRODUCT IN LIFE SUPPORT SYSTEMS.

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As used herein

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