



UP002601-0102

Product Update

Errata to SCC/ESCC User
Manual UM010901-0601

INTRODUCTION

This Errata clarifies information presented on Page 2-11 of the SCC/ESCC User's Manual, Publication Number UM010901-0601.

2.3.2 Z85SX30 Write Cycle Timing

Second paragraph should read:

Historically, the NMOS version latched the data bus on the falling edge of /WR.

Figure 2-6 Z85X30 Write Cycle Timing

NOTE: Should read as follows

Dotted line is ESCC and SCC. Please refer to individual Product Specifications for clarification.

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