Z86017/Z16017/Z86M17

PCMCIA Adapter Chips

Reference Manual Addendum

RM001201-0601

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CHAPTER 1

New Features

The Z86017/Z16017 are general purpose PCMCIA adapter chips used on the card's side of the interface. The two revisions of the chip are backward compatible, that is: Z16017 is pin to pin compatible with Z86017 and can replace it, but not vice versa. Z86017 is the earlier revision and lacks some features implemented in Z16017. Those features implemented in previous revision of silicon are described in the Reference Manual (document # UM95HDD0101). The features included in this addendum are implemented in the latest revision of the silicon.

Those features are:

1.Revision number register (address 24H) contains 40H. Previous revisions contained 20H for Z16017 and 10H for Z86017. This value should be written into the register 23H in order to unlock registers 1FH, 28H, 2AH-2FH.

2. A new feature added to the chip in the latest (Z16017) rev is that by setting to 1 bit 7 in register 3 (Interface Configuration Register) the user can change the number

of clock periods per wait state. In previous revs it could be set only to 3,5,or 7 clock periods. New numbers are presented in Table 1.

TABLE 1.

Reg03[7]	Reg10[7,6]	Tpcmclkin
X	00	00 (no wait state)
0	01	3xTpcmclkin
0	10	5xTpcmclkin
0	11	7xTpcmclkin
1	01	2xTpcmclkin
1	01	3xTpcmclkin
1	11	4xTpcmclkin

3. The data which is being transferred from/to PCMCIA can be 8or 16 bit wide. Accordingly the data transfer through Z16017 will look as it shown in Table 2.

TABLE 2.

CE1*	CE2*	PA[0]	PRD*	PWR*	PDH	PDL	LDH	LDL
L	L	X	L	H	LDH	LDL	LDH	LDL
L	H	0	L	H	zz	LDL	xx	LDL
L	H	1	L	H	zz	LDH	LDH	xx
H	L	X	L	H	LDH	zz	LDH	xx
L	L	X	H	L	PDH	PDL	PDH	PDL
L	H	0	H	L	xx	PDL	xx	PDL
L	H	1	H	L	xx	PDH	PDH	xx
H	L	X	H	L	PDH	xx	PDH	xx

If host is 8 bit wide (bit 5 in CCR1 is set to a 1) the transfer will look as follow in Table 3.

TABLE 3.

CE1*	CE2*	PA[0]	PRD*	PWR*	PDH	PDL	LDH	LDL
L	H	0	L	H	zz	LDL	LDH	LDL
L	H	1	L	H	zz	LDH	LDH	LDL

TABLE 3.

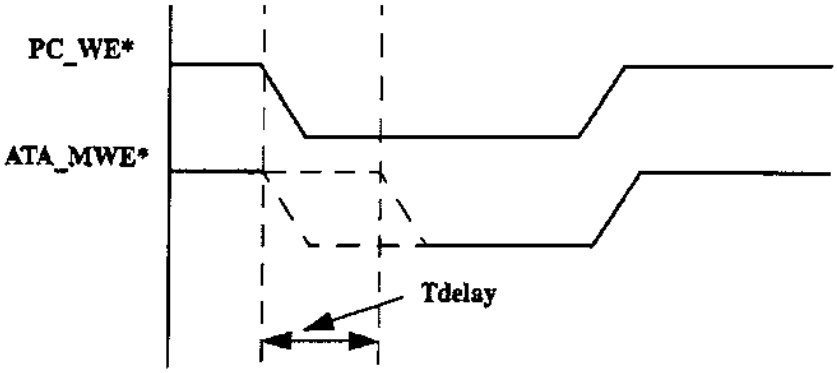
CE1*	CE2*	PA[0]	PRD*	PWR*	PDH	PDL	LDH	LDL
L	H	0	H	L	xx	PDL	PDH	PDL
L	H	1	H	L	xx	PDL	PDL	PDL

Abbreviation used in Table 2 and 3:

CE - PCMCIA Card enable
PA - PCMCIA Address
PRD - PCMCIA Read (Memory or I/O)
PWR - PCMCIA Write (Memory or I/O)
PDH - PCMCIA Data High (bits [15:8])
PDL - PCMCIA Data Low (bits [7:0])
LDH - Local Data High (bits[15:0])
LDL - Local Data Low (bits[7:0])
* - the signal is active when Low
zz - tristated
xx - don't care

4. A feature for the Z16M27 version only. Setting bit 3 in register 28H to 1 will allow delay of the leading edge of ATA_MWE* signal by Tdelay – (75-100) nS (1,5-2 Tpcmclkin), without delaying trailing edge.
The access will look as shown in Fig.1

FIGURE 1.



CHAPTER 2 *Errata*

The following information is missing from the Reference Manual (document # UM95HDD0101).
1.Programming of the EEPROM through PCMCIA.

EEPROM REGISTERS

EEPROM Address Register (Address xx8H or 7F0H)

TABLE 4.

Bit number	Bit name	Description
[7:0]	Address	EEPROM address when written to.

EEPROM Data Register (Address xxAH or 7F2H)

TABLE 5.

Bit number	Bit name	Description
[7:0]	Data	Data to be written or read from EEPROM

EEPROM Command Register (Address xxCH or 7F4H)

TABLE 6.

Bit number	Bit name	Description
[7:0]	EEPROM command	Valid command could be found in Table 5

TABLE 7.

Hex code	Command name
A8	Read EEPROM
AA	Write EEPROM
AB	Erase EEPROM to FF H
AC	Disable EEPROM write
AD	Enable EEPROM write

Please consult appropriate EEPROM Data book in order to verify how long will it take to read/write byte or block of data.

CHAPTER 3

What to look for

In this chapter we will give the answer to the most frequently asked question.

Q. How to put chip in the PCMCIA Memory or I/O mode?

A. Here is the example of programming of the EEPROM which can be used to put chip in PCMCIA mode with one window set for Memory accesses and another one for I/O accesses.

Address 00, Interface Configuration Register 0.

TABLE 8.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	1	1	0	0	1	0

Bit 7 if set to 1, enables pin ATA_PDIAG/ATA_BHE/RING to be used as a Byte High Enable (BHE) output, polarity is controlled by bit 0 in register 2FH.

Bit6 set to 0 since there is no local processor to be present on the card.

Bit 5 set to 1 to enable PCMCIA interrupt to be controlled by ATA_IREQ.

Bit 4 set to 1 to enable PC_RDY//BSY//IRQ/HINT to reflect status of the chip before host has written Configuration Index to CCR0.

Bit 3.2 both are set to 0, and mode of operation of the chip will be defined by state of the PC_HOE pin during Power-On-Reset.

Bit 1,0 the clock for the EEPROM interface (EE_SK) is set to PC_MCLKIN/16. PC_MCLKIN = 20MHz, EE_SK = 20MHz/16 = 1.25MHz, this will give Tperiod = 0.8 uS, which should be okay for almost all EEPROM. If user experienced trouble with this value (EEPROM write/read is not consistent) he can change this setting to 01 - divide by 64 or 00 - divide by 128.

Address 01, Interrupt Enable Register

TABLE 9.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	0	0	0	0	0	0

Bit 7 set to 1 to enable PC_INPACK to be generated when card is accessed.

Bit 6 set to 0 since where is no need to override bits [1,0] in register 00.

Bit 4 set to 0 since there is no need to have memory on the card to be write_protected.

Bits[3:0] are nor used.

Address 02..04 are not used, they have to be set to 00.

Address 05, PCMCIA CCR Base Register

TABLE 10.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	1	0	0	0	0	0

Sets up start address for PCMCIA Configuration Register Base Address at 200H.

Address 06..09 are not used, set them to 00.

Address 0A..0D PCMCIA Configuration Registers must be programmed accordingly to user's application.

Address 10, Window 1 Control Register

TABLE 11.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	1	0

Bits [7,6] number of Tpcmclkin per wait-state is 3.

Bit 5 ATA_HCS0 is used as external chip_select signal.

Bit 4 local address comparator is disabled, and the card will respond to all PCMCIA accesses when both PC_CE1 and PC_CE2 are active.

Bit 3 there is no two card in the system at the same address.

Bit 2 no byte swapping are needed

But 1 the card will be accessed as a memory device through this window.

Bit 0 window 1 is enabled.

Address 11..13 are not used, since bit 4 in register 10 is set to 1, set registers 11..13 to 00.

Address 14, Window 2 Control Register.

TABLE 12.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	0	0	0	0	0	0

Bits [7,6] number of Tpcmclkin per wait-state is 3.

Bits [7,6] number of Tpcmclkin per wait-state is 3.

Bit 4 local address comparator is disabled, and the card will respond to all PCMCIA accesses when both PC_CE1 and PC_CE2 are active.

Bit 3 there is no two card in the system at the same address.

Bit 2 no byte swapping are needed

But 1 the card will be accessed as an I/O device through this window.

Bit 0 window 2 is enabled.

Address 15..17 are not used, since bit 4 in register 14 is set to 1, set registers 15..17 to 00.

Address 18, Window 3 Control Register.

TABLE 13.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	1

Bit 0 Window 3 is disabled, rest of the bits should be set to 0.

Address 19..1D are not used, set them to 00.

Address 1E, Valid EEPROM register.

In order for EEPROM to be valid this register shall have 1CH.

Address 1F, PCMCIA I/O Event Indication Register.

Address 20..23 are not used, set them to 00.

Address 23, Revision Control Register.

When this register has been written with the value read from Register 24, Revision Number Register, it will "unlock" registers 1F,28, 2A...2F.

Here are the additional errata and more detailed description of some features of the 16017.

1. Page 2-2

Table 2-2

ICR_2[1:0]	Description
...	
11	PCMCIA ATA mode.

1. Page 3-3:
Bits 1-0 should read:

Bit 1	Bit 0	
0	0	Slowest clock. Clock-in divided-by 128
0	1	Clock-in divided-by-64
1	0	Clock-in divided-by-16
1	1	Clock-in divided-by-4

2. Page 3-9:
Address: SELECT 04H

Bit 5 EN_DIS_RST Disable PCMCIA reset. This bit is active when set to 1. Disables PCMCIA reset to effect Local Bus Devices.
Does not have effect on the chip itself.

Page 3-11:

Address: SELECT 06H

Bit 6 this bit is set to 1 after Revision Control Register (Address 23H) has been written with the Revision Number.
Revision number for 16017 SI1868 is 40H.

Page 3-13
Address: SELECT 10H

Bits 7-6
01 = 3xTpmckin

The following will be the same for registers 11H, 15H, 19H, and 12H, 16H, 1AH, and 13H, 17H, 1BH accordingly.

Address 11(15, 19) H

Bits 7-0 Least Significant Byte of the starting Address for Window 1(2,3)

Address 12(16,1A) H

Bits 2-0 Bits 8,9 and 10 of the Starting Address for Window 1(2,3)

Bits 6-4 Bits 8,9 and 10 of the Ending Address for Window 1(2,3)

Address 13(17,1B) H

Bits 7-0 Least Significant Byte of the Ending Address for Window 1(2,3)

EEPROM Address/Status Register (Address 7F0)

Bits 7-0 EEPROM Address when written to.

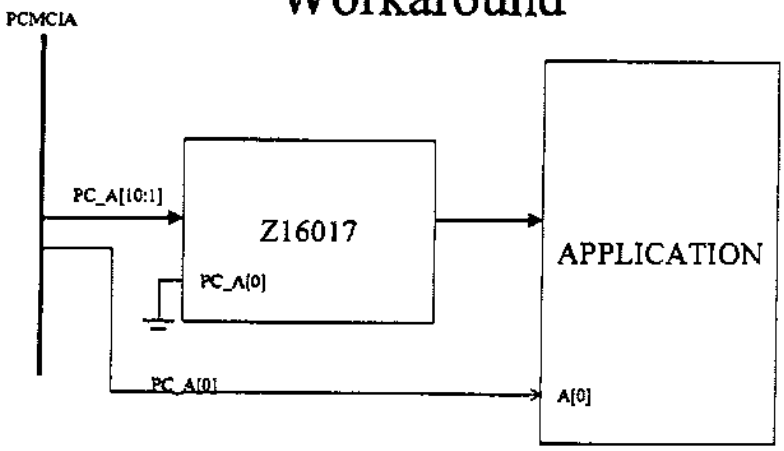
Bit 0 EEPROM Write is in progress. This bit is set to 0 when Command EEPROM Write is in progress. When Command is completed it is set to 1. It is set to 1 on POR .

Bit 1 Read Valid. This bit is set to 1 when Read or Enable EEPROM or Disable EEPROM command is completed. It is set to 0 on POR.

Bits 7-2 Reserved.

The following is the workaround to make z16017 work in 8-to-8 bit environment

Workaround



Regards, and sorry for mistakes.

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