Crystal Oscillator for Embedded Modems

Specify the Correct Crystal for Z02201/Z02215Z02922

INTRODUCTION

Specifying a crystal for a modem system requires careful thought and detailed verification. Voltage and temperature effects on the crystal and internal gain element, combined with layout parasitics, can cause errors in the clock rate of the circuit. If too large, these errors will bring the baud rate outside ITU specifications (V.22bis, etc.). Careful testing of the final system is required to guarantee that such discrepancies are not overlooked until seen by customers as improper modem operation in the field. The recommended circuits, component selections, and layout help the process of choosing the right starting point in this process.

CRYSTAL OSCILLATOR DESIGN

The crystal oscillator circuit is designed to use a parallel resonant crystal and two capacitors in conjunction with the internal inverter (gain element) between the XTAL and EXTAL pins on the Z02201 or Z02922. Place a 100K Ohm resistor in parallel with the crystal to provide a DC path for startup of the oscillator. These external passive components operate with the internal inverter to produce the data pump clock signal.

The clock frequency is divided down to produce the baud rate for the transmit side of the Z02201 or Z02922. Capacitors (C_1 and C_2) are placed from XTAL and EXTAL to ground, respectively, to achieve this oscillation. Figure 1 illustrates the circuit.

Alternately, a complete clock oscillator can be used to drive the EXTAL pin of the inverter. The complete oscillator will probably be more expensive, and produce more EMI radiation, since it will usually be specified with higher drive requirements than the internal oscillator.

In either case, the oscillator must be accurate to within 100 Parts Per Million (ppm) or 0.01% of 24.576 MHz, in order to meet the baud rate requirements for transmission (2400 baud for V.22bis, or 1200 baud for V.22 and Bell 212A). This requirement must be true despite variations in power supply voltage, temperature, capacitor variation, and other application or environmental variables.

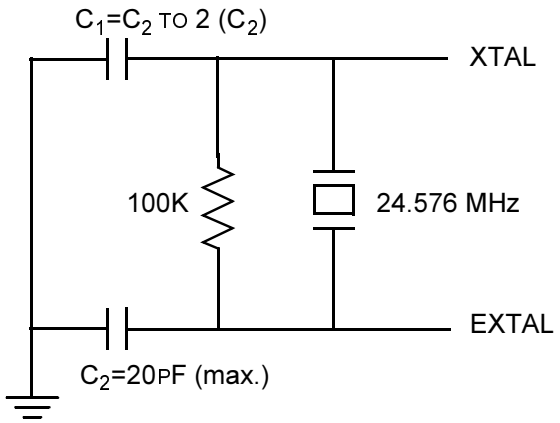

Figure 1. Crystal Oscillator Circuit

CRYSTAL BACKGROUND

Crystals are normally specified and tested by the manufacturer in terms of initial accuracy, drift over temperature, and aging or shift with time. These specs are verified in a test setup with a specific load capacitance. The circuit conditions in the actual oscillator only approximate this capacitance, resulting in board parasitic capacitances and tolerance variations in C_1 and C_2.

CRYSTAL CHARACTERISTICS

The equivalent circuit of the crystal is illustrated below in Figure 2.

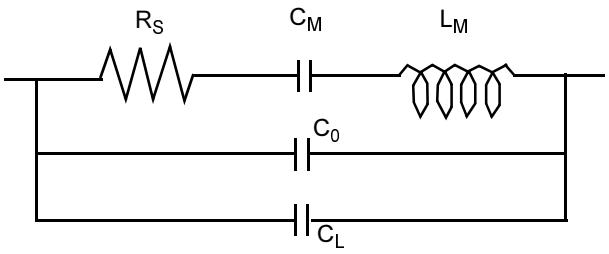

Figure 2. Crystal Equivalent Circuit

C_0 is the electrical shunt capacitance of the package and leads for the device. The motional parameters L_M, C_M, and R_S are due to the vibrating mass, physical elasticity, and damping losses, respectively, of the crystal operating near its resonant frequency.

C_0, paralleled by load capacitance C_L, is illustrated as follows:

$$C_T = C_0 + C_L$$

$$f_{seriesresonant} = f_s = \frac{1}{2\pi\sqrt{C_M \times L_M}}$$

$$f_{parallelresonant} = f_p = \frac{1}{2\pi\sqrt{\frac{C_O C_M L_M}{C_O + C_M}}}$$

When loaded, the circuit resonates between f_s and f_p at:

$$f_{loadresonant} = f_l = \frac{1}{2\pi\sqrt{\frac{C_T C_M L_M}{C_T + C_M}}}$$

Given f_s (also very near f_p) and C_m:

$$L_m = \frac{1}{4\pi^2 f_s^2 C_M}$$

Then the Q is:

$$Q = \frac{2\pi f_S L_m}{R_S}$$

RECOMMENDATION

Crystal resonator specs recommended by ZiLOG for use with the Z02201 or Z02922 are as follows:

Both KDS America (*714-557-7833; www.kdsamerica.com*) and Fox Electronics (*941-693-0099; www.foxonline.com*), for example, supply crystals to these specifications. The specifications are an attempt to take into account variations in tolerance of load and parasitic capacitances, and inverter gain with supply and temperature.

Table 1. Suggested Crystal Specifications Based on C_1=C_2=20pF*, C_0=2 pF

Parameter	Value×
Temperature Range (Commercial) Temperature Range (Industrial)	0°C to +70°C –40°C to +85°C
Nominal Frequency @ 25°C	24.576 MHz
Frequency Tolerance @ 25°C	±20 ppm
Temperature Stability @ 0°C to 70°C	±25 ppm
Calibration Mode	Parallel Resonant
Shunt Capacitance (C_0)	4 pF max.
Load Capacitance	15 pF
Drive Level	1.5 mW max.
Aging, per Year Max.	±5 ppm
Oscillation Mode	Fundamental
Series Resistance	25 Ohms max.
Q	70K
*Includes pin parasitics	
Suggested reading: IEEE JSSC p222-228 April 1980 IEEE JSSC p744-783 June 1988	

VERIFYING OPERATION

Operation of the final circuit, in its layout and environmental conditions, should be carefully verified with an accurate and properly guardbanded frequency counter. Doing so assures system compliance with ITU specs (100 ppm). In order to avoid loading the XTAL or EXTAL terminals with the parasitic input capacitance of the frequency counter, the EYECLK can be monitored instead of the crystal oscillator directly. The eyeclock rate should be 1.536 MHz to within the desired tolerance.

IMPACT OF FREQUENCY INACCURACY

The consequence of being outside the ITU specified frequency will typically not be catastrophic in the application. In fact, without explicitly checking the frequency with an accurate frequency counter, an inaccuracy may persist undetected even into production. This situation occurs because most modems are designed to handshake and receive data properly, even with a modem transmitting at a baud rate outside ITU (V.22bis, etc.) specs. The error may then be discovered in the field by the presence of bursts of data reception errors, or an inability to handshake properly when operating with modems of less robust operating ability. In such a case, the fault should be placed on the modem with inaccurate (and out of specification) transmission baud rate, dependent on the clock oscillator.

GUARANTEEING FREQUENCY COMPLIANCE

It is important to make sure the clock frequency is accurate within the 100 ppm specs. The total load capacitance is the series combination of C_1 and C_2, added to the effective stray capacitance C_{STRAY} between the inverter input and output, typically yielding about 3 to 5 pF.

$$C_L = \left(C_{STRAY} + \frac{C_1 C_2}{C_1 + C_2} \right)$$

If the frequency of oscillation is low, reducing the capacitors (C_1 and C_2) will raise the frequency. Increasing their value will reduce the frequency of oscillation.

The tolerances of the crystal resonators must be sufficiently tight to guarantee frequency conformance to the overall system.

In order to minimize the effects of parasitic capacitance, all traces, especially XTAL and EXTAL, should be as short as possible. Traces should also be physically separated and shielded if possible, avoiding any overlap, or parallel spacing that is too close.

Characterization of the final design and layout should be done over temperature and power supply voltages, since the gain of the inverter and crystal specs are dependent on these variables.

The goal is guaranteeing frequency accuracy by design in cooperation with sourcing policies, avoiding the need for incoming inspection, and final test procedures.

CONCLUSION

The overall frequency of the entire clock oscillator must be within 100 ppm in the modem application, despite all circuit, component, environmental and layout variables. This frequency sets the transmission baud rate. Therefore, the crystal must be specified tightly enough for the overall system to remain in specification.

Pre-Characterization Product:

The product represented by this CPS is newly introduced and ZiLOG has not completed the full characterization of the product. The CPS states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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