Application Note

Set Up a PLL Loop Filter on the eZ80F91 MCU

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Abstract

This document provides information that will help an application developer effectively use the eZ80F91 MCU's on-chip Phase-Locked Loop (PLL) feature as a system clock source. The included circuits and procedures can help the developer select the appropriate external loop filter components, code the application's PLL initialization sequence, and verify proper PLL operation.

eZ80Acclaim*Plus!*™ Flash MCU Overview

eZ80Acclaim*Plus!*™ on-chip Flash Microcontrollers are an exceptional value for customers designing high performance, 8-bit MCU-based systems. With speeds up to 50 MHz and an on-chip Ethernet MAC, designers have the performance necessary to execute complex applications quickly and efficiently. Combining Flash and SRAM, eZ80Acclaim*Plus!*™ devices provide the memory required to implement communication protocol stacks and achieve flexibility when performing in-system updates of application firmware.

The eZ80Acclaim*Plus!*™ Flash MCU can operate in full 24-bit linear mode, addressing 16 MB without a Memory Management Unit. Additionally, support for the Z80-compatible mode allows Z80/Z180 customers to execute legacy code within multiple 64-KB memory blocks with minimum modification. With an external bus supporting eZ80, Z80, Intel and Motorola bus modes and a rich set of serial communications peripherals, designers have several options when interfacing to external devices.

Some of the many applications suitable for eZ80Acclaim*Plus!*™ devices include vending machines, point-of-sale terminals, security systems, automation, communications, industrial control and facility monitoring, and remote control.

Definitions

- Loop Bandwidth

  The loop bandwidth, BW, is the effective PLL control loop range. It determines the PLL control loop's ability to track loop perturbations and noise. The loop can only track noise within the bandwidth of the loop. Therefore, a wider bandwidth is preferable.

- Phase Margin

  Phase margin is a measure of real-time PLL frequency control loop stability. Higher phase margin equates to better overall control loop performance. As the phase margin increases, frequency lock time also increases. Increased lock time is not a concern for applications using the eZ80F91 MCU.

  The Loop Bandwidth and Phase Margin values defined in the tables in the section that follows show the potential impact of different Loop Filter Component selections on overall PLL performance.

Discussion

The eZ80F91 PLL is part of the System Clock Generation block, which includes an on-chip oscillator, PLL circuit, and system clock source selection logic, as diagrammed in Figure 1.

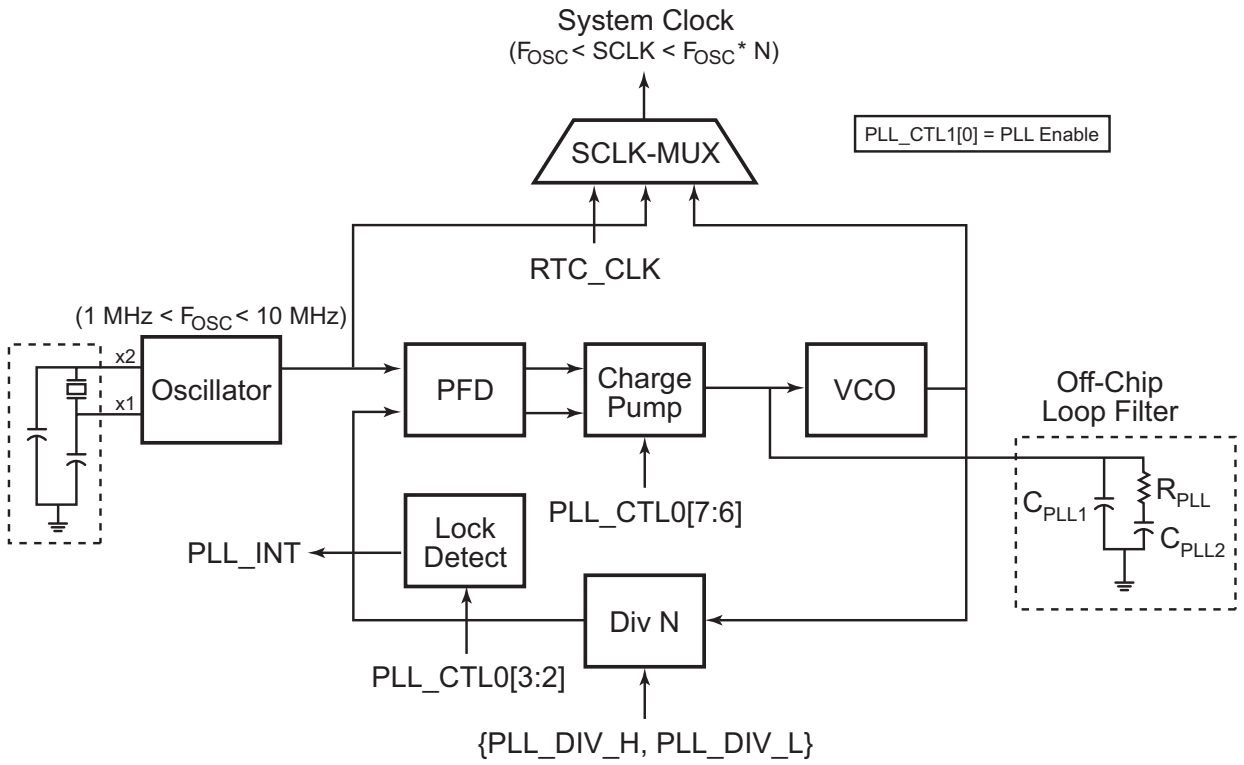

Figure 1. System Clock Generation Block

The PLL is a programmable frequency multiplier designed to generate the 50-MHz system clock (SYSCLK) from a variety of lower-frequency reference sources. The PLL requires the user to select an off-chip PLL reference frequency, the loop filter components, and to set the PLL setup and control registers based on off-chip component selections. User selectability of the multiplier source, as opposed to using a fixed reference, is offered to accommodate component constraints set by cost points, stocking approach, or performance goals. PLL programmability is not intended to generate SYSCLK frequencies other than 50 MHz.

Note: *Operation at frequencies other than the design target of 50 MHz are not guaranteed to function in all cases. The PLL's F_{out} value should be defined as 50 MHz for guaranteed operation across the device's complete temperature and silicon-processing parameter range. Zilog production testing confirms that the PLL functions at an F_{out} value equal to 50 MHz.*

The eZ80F91 PLL is a third-order phase lock loop that utilizes an on-chip oscillator with an external crystal that functions as a reference, a Phase Frequency Detector (PFD), a charge-pump loop filter with external loop filter passive components, a Voltage Controlled Oscillator (VCO), and a frequency divider (programmable downcounter). The eZ80F91 MCU's primary oscillator generates the PLL reference. The oscillator must be driven by a 1–10 MHz fundamental frequency crystal (see Figure 2 and Table 1). Alternatively, the X_{IN} input pin can also accept a CMOS-level clock input signal. If an external clock generator is used in the design, the X_{OUT} pin should remain unconnected.

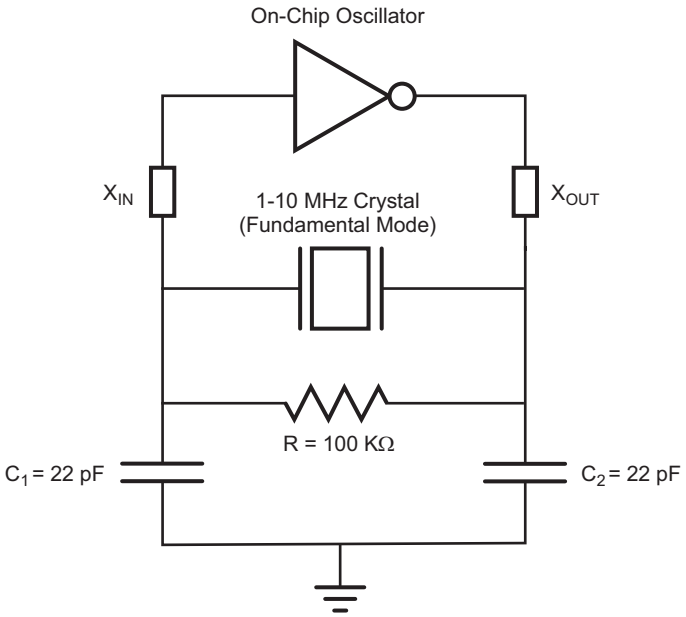

Figure 2. 1–10 MHZ Crystal Circuit

Table 1. Crystal Specifications

Parameter	1 MHz	10 MHz	Units	Comments
Frequency	1	10	MHz	
Resonance	Parallel			
Mode	Fundamental			
Series Resistance (RS)	750	35	Ω	Maximum
Load Capacitance (CL)	13	30	pF	Maximum
Shunt Capacitance (CO)	7	7	pF	Maximum
Drive Level	1	1	mW	Maximum

The charge-pump loop filter filters the PFD phase error signal to create the DC voltage that drives the VCO. The charge pump is a selectable current source with four programmable values: 1.5 mA, 1 mA, 500 µA, and 100 µA. The selected current drive is sinked/sourced onto the loop filter pin according to the error (or difference) between the falling edges of the PFD output signals. Ideally, when the PLL is locked, there are no control loop errors (error = 0) and no current is sourced/sinked onto the off-chip loop-filter. In general, the higher the charge pump current, the less sensitive the PLL is to noise disturbing the loop filter node; for example, power supply noise.

The external loop filter passive components include a series capacitor, C_{PLL2}, and a series resistor, R_{PLL}, in parallel with a capacitor, C_{PLL1} (see Figure 1). The loop filter operates in the 1–10 MHz PLL reference frequency range. Therefore, high-performance components are not required. The components should be placed as close as possible to the Loop Filter pin and achieve a common Ground with the PLL_V_{SS} pin.

The loop filter bandwidth and phase margin define overall PLL noise and frequency stability control. Zilog recommends using as high a PLL reference frequency as possible (for example, 10 MHz) to create the widest loop filter bandwidth and largest phase margin.

The divider is a user-programmable downcounter. The function of the divider is to divide the frequency of its input signal (VCO_{OUT}) by a programmable factor N and supply the result to the PFD circuit. Factor N is defined as the target SYSCLK frequency ÷ reference (X_{IN}) frequency. Div N is programmed by the PLL_DIV_L and PLL_DIV_D registers.

Table 2 contains acceptable values for different reference source frequencies. See Table 3 for the values that Zilog recommends as starting points for components and for PLL setup parameters for the charge-pump currents.

Table 2. Loop Filter Circuit Values

X_{IN} (MHz)	N (div)	SYSCLK (MHz)	R_{PLL} ± 10%	C_{PLL2} ± 10%	C_{PLL1} ± 10%	Charge Pump Current	Phase Margin (Degrees)	BW
1	50	50	1 k	33 nF	100 pF	100 µA	73.1	8 KHz
			270	0.10 µF	220 pF	500 µA	74.6	11 KHz
			150	0.15 µF	220 pF	1.0 mA	73.8	12 KHz
			150	0.10 µF	220 pF	1.5 mA	73.6	18 KHz
3.579545	14	50.1	1 k	10 nF	47 pF	100 µA	73.8	29 KHz
			220	47 nF	220 pF	500 µA	75.4	27 KHz
			150	47 nF	220 pF	1.0 mA	74.5	43 KHz
			100	68 nF	330 pF	1.5 mA	74.0	43 KHz
8	5	40	510	15 nF	100 pF	100 µA	74.4	41 KHz
			100	68 nF	220 pF	500 µA	73.5	40 KHz
			100	33 nF	220 pF	1.0 mA	72.4	80 KHz
			100	22 nF	220 pF	1.5 mA	71.7	121 KHz
10	5	50	510	15 nF	100 pF	100 µA	74.4	41 KHz
			100	68 nF	220 pF	500 µA	73.5	40 KHz
			100	33 nF	220 pF	1.0 mA	72.4	80 KHz
			100	22 nF	220 pF	1.5 mA	71.7	121 KHz

Notes:
1. Place the loop filter components as close as possible to the package pins. Provide a common analog ground with the PLL device Ground pin.
2. A charge pump current of 500 µA is the recommended starting point.
3. Operation of the PLL for output frequencies other than 50 MHz is not guaranteed over the entire standard temperature range for all devices. The 40-MHz SYSCLK in this table is provided for reference. Zilog production testing confirms that the PLL functions at a SYSCLK value equal to 50 MHz.
4. Zilog recommends interpolating the loop filter component values between the given X_{IN} frequencies.

Table 3. Recommended Values

Parameter	Value	Units
X_{IN}	10	MHz
N	5	
SCLK	50	MHz
R_{PPL}	100	Ω
C_{PLL2}	47	nF
C_{PLL1}	220	pF
Charge Pump Current	500	µA

Verifying PLL Operation

For most applications, the component values in Table 2 for a 500-µA charge-pump current are the best configuration for the defined X_{IN} frequencies. To test the PLL setup, the following must occur:

- The PLL must lock
- The PLL must lock within the defined lock criteria of 8 or 16 reference frequency cycles. To ensure that the PLL locks correctly:
  - Check the device and PLL_V_{DD}
  - Check the reference frequency
  - Check the loop filter components
  - Use 16 cycles as the lock criteria
  - Increase the loop filter bandwidth and/or phase margin
- Following lock and PLL SYSCLK source selection, the PHI pin must have the correct frequency. To ensure that the PHI pin frequency is correct:
  - Check the PLL_DIV value
  - Check the reference frequency
- During PLL SYSCLK source operation, the PLL must not generate unlocked interrupts, as such:
  - Check all of the above items
  - System V_{DD}, PLL V_{DD}, and Ground should be checked for noise

Initialization Sequence

The following steps provide an example of the on-chip initialization sequence.

1. POR/System Reset
   a. CLK_MUX defaults to External Crystal Oscillator PLL reference frequency.
   b. PLL_ENABLE defaults to DISABLED.
   c. All eZ80F91 registers can be accessed as defined in the *eZ80F91 Product Specification* (PS0192).
2. Define PLL Interrupt Service Routines
   a. PLL interrupts default on reset to Priority 3.
   b. Both the Locked and Unlocked PLL interrupts require ISR routines.
3. Program PLL Registers
   a. PLL_DIV_L
   b. PLL_DIV_H must be set to `00h`. Only the lower PLL_DIV six bits are valid for the reference frequency range of 1–10 MHz; PLL_DIV is WRITE ONLY; READs return a `00h`.
   c. CHRP_CTL is as defined in Table 2.
   d. LDS_CTL is set to 8 or 16 cycles of 20-ns duration, default is 8 cycles; 400-ns options are not supported on the eZ80F91 MCU.
4. Enable PLL Operation
   a. INT_LOCK_EN must be set to Enabled 1.
   b. INT_UNLOCK_E must be set to Disabled 0.
   c. PLL_ENABLE must be set to Enabled 1.
5. On PLL-Locked Interrupt
   a. CLK_MUX must be set to PLL 01.
   b. INT_LOCK must be set to Read to clear.
   c. INT_LOCK_EN must be set to Disabled 0.

d. INT_UNLOCK_E must be set to Enabled 1.

6. Execute application code at PLL F_{OUT}.

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