

Errata for Z85C30 Silicon

The errata listed in Table 1 highlights the issue and workaround for Zilog's Z85C30 silicon for all date codes and packages.

Item No	Issue	Description
1	data FIFO, the data on D7- D0 may become invalid	In the Z85C30 Read/Write timing table, the D7-D0 data from the receive data FIFO should remain valid until the /RD pin is deas- serted. However, if your application timing uses a /RD cycle lon- ger than two PCLK cycles to read the receive FIFO, the data on D7-D0 may become invalid.
		Workaround The following two options are available:
		• Latch the data on D7-D0 before the end of the second PCLK cycle after /RD is asserted.
		• Use the Z85230 in the application instead of the Z85C30.

Table 1. Errata for Z85C30 Silicon



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