18V Input Voltage Step-Down Synchronous DC/DC Converter

FEATURES

- **Built-in transistors**
- **Operating Input Voltage Range**: 4.5 V ~ 18.0 V
- **Output Voltage Range Externally Set**: 1.0 V – 12 V
- **Output Current**: up to 2.2 A
- **Reference Voltage**: 0.8V ± 1.5%
- **Oscillation Frequency**: 500 kHz
- **Maximum Duty Cycle**: 79%
- **Soft Start:** 2.8 ms internal or set by external capacitor
- **Protection:** High and Low side Over-current, V_{OUT} and L_X short circuit protection, Under-voltage Lockout, and Thermal Shutdown
- **Small Package:** SOP-8FD

APPLICATION

- Digital home appliances
- Office automation equipment
- Car accessories power supplies
- Various portable equipment

DESCRIPTION

The IXD3248 IC is an 18 V PWM mode bootstrap synchronous step-down DC/DC converter with built-in N-channel driver transistors.

With an input voltage range from 4.5 V to 18 V and a maximum output current of 2.2 A, the IXD3248 is suitable for power supplies used in home appliances and car accessories.

The IXD3248 has a 0.8 V reference voltage that allows setting the output voltage from 1.0 V to 12 V by external resistors.

Small ceramic capacitors are required for IC normal operations.

The soft start time is internally set to 2.8 ms and it can be adjusted using the external capacitor.

Under Voltage Lockout (UVLO) forces internal driver transistors OFF when input voltage falls below 3.8 V typical.

The IXD3248 includes over current protection, V_{OUT} and L_X pin short-circuit protection, V_{OUT} overvoltage protection, and thermal shutdown.

The IXD3248 is available in SOP-8FD small package.

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TYPICAL APPLICATION CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTIC

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage	V_{IN}	– 0.3 ~ 20.0	V
EN Pin Voltage	V_{RB}	– 0.3 ~ 20.0	V
L_X Pin Voltage	V_{LX}	– 0.3 ~ V_{IN} or +20.0[1]	V
BST Pin Voltage	V_{BST}	V_L – 0.3 ~ V_L + 20; V_{LX} – 0.3 ~ V_{LX} + 5.5	V
V_L Pin Voltage	V_L	– 0.3 ~ V_{IN} +0.3 or +5.5[2]	V
FB Pin Voltage	V_{FB}	– 0.3 ~ +5.5	V
SS Pin Voltage	V_{SS}	– 0.3 ~ +5.5	V
Lx Pin Current	I_{LX}	±5	A
V_L Pin Current	I_{VL}	85	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{OPR}	– 40 ~ + 105	^0C
Storage Temperature Range	T_{STG}	– 50 ~ +125	^0C

ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise specified, Ta = 25 ^{0}C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
Input Voltage Range	V_{IN}	If V_{IN} ≤ 7 V, V_{OUT} = 3.3 V; if $_{VIN}$ ≥ 7 V, V_{OUT} = 5 V	4.5	-	18.0	V	①
FB Voltage	V_{FB}	SS pin - open	0.788	0.800	0.812	V	②
FB Voltage Temperature Characteristics	$\dfrac{\Delta V_{FB}}{V_{FB} * \Delta t_{OPR}}$	-40^0C ≤ T_{OPR} ≤ 105^0C		±40		ppm/^{0}C	②
Maximum Output Current	I_{OUT_MAX}		2.2[1]			A	①
Supply Current	I_Q	V_{IN} = V_{EN} = 18 V, V_{FB} = 0.9 V		0.76	1.1	mA	①
Standby Current	I_{STB}	V_{IN} = 18 V, V_{EN} = 0 V, V_{FB} = OPEN		38	51	µA	③
Oscillation Frequency	f_{OSC}	V_{FB} = 0.7 V, V_{SS} = OPEN	450	500	550	kHz	②
Maximum Duty Cycle Ratio	D_{MAX}	V_{FB} = 0.7 V, V_{SS} = OPEN	74	79	-	%	②
UVLO Detection Voltage	V_{UVLOD}	V_{EN} = 2V, V_{FB} = 0.9 V[2]	3.50	3.80	4.45	V	④
UVLO Release Voltage	V_{UVLOR}	V_{EN} = 2V, V_{FB} = 0.9 V[3]	3.55	3.90	4.50	V	④
Low Side Current Limit	I_{LIMLS}	V_{OUT} = 4.5 V (Forced), L_X pin Current	2.1			A	⑦
Integral Protection Time (Type A)	t_{PRO}	V_{FB} = 0.9 V, I_{LX} = I_{LIMLS}[4]	0.4	1.1	1.8	ms	⑤
Internal Soft-Start Time	t_{SS}	V_{IN} = 12 V, V_{EN} = 2 V, V_{FB} = 0.72 V, V_{SS} = OPEN[5]		2.8		ms	②
SS pin Current	I_{SS}	V_{SS} = 0, V_{LX} = V_{FB} = OPEN	2	4	6	µA	⑥
SS Threshold Voltage	V_{SSTH}	V_{FB} = 0.72 V, V_{SS} = OPEN[6]	1.2	1.8	2.4	V	②
OVP Detection Voltage	V_{OVPD}	V_{FB} = Sweep 0.788 – 1.2 V, V_{SS} = OPEN		0.9	1.2	V	②
Efficiency [7]	EFFI	V_{OUT} = 5 V, I_{OUT} = 0.7 A		93.8		%	⑧
L_X "H" ON Resistance	R_{LXH}			0.12[8]		Ω	④
L_X "L" ON Resistance	R_{LXL}			0.12[8]		Ω	④
EN "H" Voltage[9]	V_{ENH}	V_{IN} = 12 V, V_{FB} = 0.9 V	1.4			V	④
EN "L" Voltage[10]	V_{ENL}	V_{IN} = 12 V, V_{FB} = 0.9 V			0.2	V	④
EN "H" Current	I_{ENH}	V_{IN} = V_{EN} = 18 V, V_{LX} = V_{FB} = V_{SS} = OPEN		16	21	µA	⑥
EN "L" Current	I_{ENL}	V_{IN} = 18 V, V_{EN} = 0 V, V_{LX} = V_{FB} = V_{SS} = OPEN	-0.1		0.1	µA	⑥
FB "H" Current	I_{FBH}	V_{IN} = 18 V, V_{EN} = 0 V, V_{FB} = 5 V, V_{LX} = V_{SS} = OPEN	-0.1		0.1	µA	⑥
FB "L" Current	I_{FBH}	V_{IN} = 18 V, V_{EN} = 0 V, V_{FB} = 5 V, V_{LX} = V_{SS} = OPEN	-0.1		0.1	µA	⑥
L_X "L" Current	I_{LXH}	V_{IN} = 18 V, V_{EN} = V_{FB} = 0 V, V_{LX} = V_{SS} = OPEN	-0.1		0.1	µA	⑥
Thermal Shutdown Temperature	T_{TSD}			150		^0C	
Thermal Shutdown Hysteresis	T_H			25		^0C	
C_L Discharge Resistance	R_{CL}	V_{IN} = 12 V, V_{EN} = 0 V, V_{LX} = 2 V, V_{FB} = V_{SS} = OPEN		300		Ω	⑥
CL Discharge Current	I_{CL}	V_{IN} = 12 V, V_{EN} = 0 V, V_{LX} = 12 V, V_{FB} = V_{SS} = OPEN		9		mA	⑥

NOTE:

Unless otherwise stated, $V_{IN} = V_{EN} = 12$ V
1. Mount conditions affect heat dissipation. Maximum output current is not guaranteed, when Thermal Shutdown starts to operate earlier.
2. Voltage when V_L pin changes state from "L" to "H" level ("H" = 4.3 ～5 V, "L" = −0.1～0.1 V), when V_{IN} sweeps 3.5 V → 4.5 V.
3. Voltage when V_L pin changes state from "H" to "L" level, when V_{IN} sweeps 4.5 V → 3.5 V.
4. Time until SS pin changes state from "H" to "L" level
5. Time until oscillations appear at L_X pin
6. Voltage at SS pin, at which oscillations appear at L_X pin
7. EFFI = {[(output voltage)×(output current)] ÷ [(input voltage)×(input current)]} ×100
8. Design value
9. Voltage at EN pin, at which V_L pin changes state from "L" to "H"
10. Voltage at EN pin, at which V_L pin changes state from "H" to "L"

PIN CONFIGURATION

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V_IN  1        8  L_X
EN    2        7  GND
SS    3        6  BST
FB    4        5  V_L
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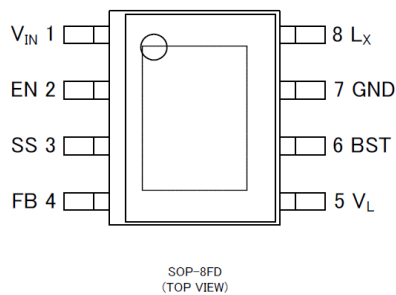
SOP−8FD
(TOP VIEW)

The dissipation pad for the SOP-8FD package should be solder-plated in recommended mount pattern and metal masking to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the pin No.7 (GND).

PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
1	V_{IN}	Power Input
2	EN	IC Enable (LOW – standby mode, HIGH – active state). Do not keep open.
3	SS	External Soft Start
4	FB	FB Voltage Monitor
5	V_L	Internal Regulator Output
6	BST	Bootstrap
7	GND	Ground
8	L_X	Switching Output

BLOCK DIAGRAM
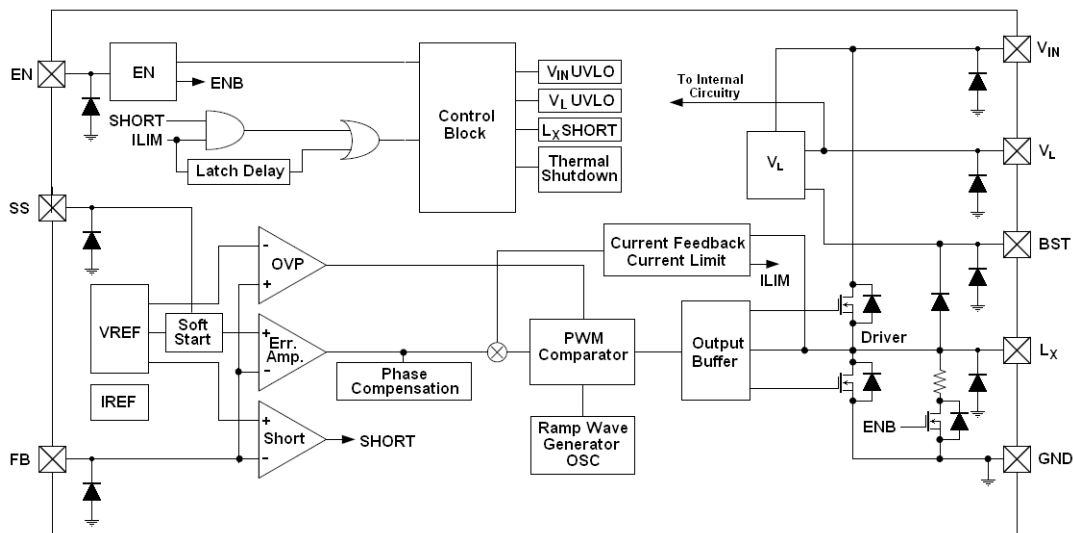
Internal diodes include an ESD protection and a parasitic diode

BASIC OPERATION

The IXD3248 controller contains an internal Reference Voltage Source, Ramp Wave Generator, Error Amplifier, PWM Comparator, Phase Compensation circuit, N-channel MOSFET Driver, Current Limiter, UVLO, Short circuit protection, Thermal Shutdown circuit, Over Voltage Protection, and other blocks (See the block diagram).

The Error Amplifier compares FB pin voltage with the internal reference voltage. The amplified difference between these two signals applies to the first input of the PWM Comparator, while ramp voltage from the Ramp Wave Generator applies to the second input. The resulting PWM pulse determines switching MOSFET's ON time. It goes through the Buffer and Driver, and it appears at the L_X pin to drive gate of the external switching MOSFET. This continuous process stabilizes output voltage.

The Current Feedback circuit monitors the N-channel MOSFET Driver transistors current at each switching cycle, and modulates output signal from the Error Amplifier to provide additional feedback. This guarantees a stable converter operation even with low ESR ceramic load capacitor.

Reference Voltage Source

The Reference Voltage Source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

Ramp Wave Generator

The Ramp Wave Generator produces ramp waveform signal needed for PWM operation, and signals to synchronize all the internal circuits. It operates at an internally fixed 500 kHz frequency.

Error Amplifier

The Error Amplifier monitors output voltage through resistive divider connected to FB pin. If the output voltage falls below preset value, the FB pin voltage becomes less than internal reference voltage and the output voltage of the error amplifier increases. This results in wider PWM pulse and respectively longer ON time for switching MOSFET to increase output voltage. The gain and frequency characteristics of the error amplifier output are fixed internally to optimize IC performance.

Current Limiting

The Current Limiting circuit monitors the current that flows through the Low side and High side of the N-channel MOSFET Driver transistors, and when over-current is detected, the current limiting function activates.

Low side current limiting

The Low side driver current limiting prohibits the High side driver transistor from turning on in an over-current condition, when the inductor current is higher than the Low side driver current limit value I_{LIMLS}. It also reduces the switching frequency f_{OSC} to accommodate higher load. Normal operation resumes after the over-current condition clears.

High side driver current limiting + Low side driver current limiting

The High side driver current limiting function turns off the High side driver transistor when the inductor peak current reaches the High side driver current limit I_{LIMHS}. Because the Low side driver current limit is less than High side driver current limit (internally set), the Low side driver current limiting function also detects the over-current state at this time. Normal operation resumes after the over-current condition clears.

Over-current latch (Type A)

The IXD3248A controller turns off the High side and Low side driver transistors when either low or high side current limits exist for more than 1.1 ms typically. After that, the L_X pin internally forced to the ground to discharge load capacitor C_L and latched in this state; however, the internal circuitries of the IC continue to operate.

To restart the controller's operation after this condition, either EN pin should be toggled H – L – H, or V_{IN} pin voltage should be set below UVLO to resume operations from soft start.

To prevent malfunctions of the over-current latch like false triggering or delayed/not triggering at over-current condition, input capacitor C_{IN} should be as close to the IC as possible.

The IXD3248A controller automatically recovers after the over-current state clears.
Low side driver current limit value I_{LIMLS} = 2.1 A (MIN.)
High side driver current limit value I_{LIMHS} = 4.1 A (TYP.)
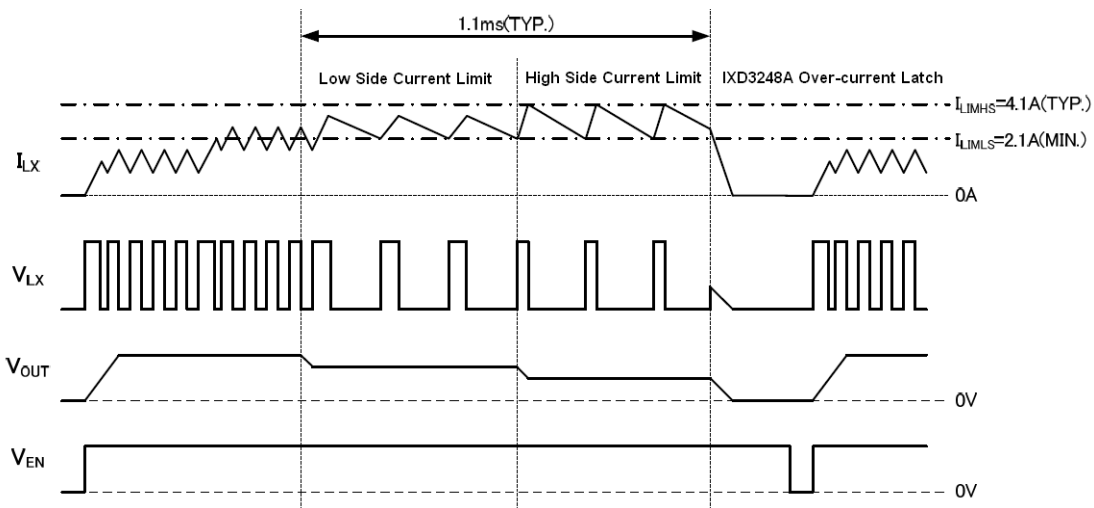
Thermal Shutdown

Thermal Shutdown circuitry monitors chip temperature to prevent IC from damage. The Thermal Shutdown circuit starts operating when the chip's temperature reaches 150^0C and turns off the N-channel MOSFET driver transistors. After that, the L_X pin internally forced to the ground to discharge load capacitor C_L.

When the temperature drops to 125^0C or less, the IC performs a soft-start to resume normal operation.

UVLO Circuit

If the V_{IN} voltage is or falls below 3.8 V, the N-channel MOSFET Driver transistors are OFF, and the L_X pin is internally forced to the ground to discharge load capacitor C_L. When the V_{IN} voltage becomes 3.9V or higher, the IC performs a soft-start and it resumes normal operation.

The soft-start initializes even when the V_{IN} voltage falls below the UVLO detect voltage for a very short time. The UVLO circuit does not cause a complete shutdown of the IC, but stops PWM pulses. Therefore, the internal circuitry remains in operation.

Bootstrap method

The bootstrap method is used to generate a voltage higher than the V_{IN} voltage to drive gate of the high side N-channel MOSFET Driver transistor.

The C_{BST} capacitor connected between the BST and LX pins charges to V_L voltage when the low side N-channel MOSFET Driver transistor is conducting, and it applies this voltage to BST pin in respect to the L_X pin to drive gate of high side MOSFET, when the low side transistor is off.

V_{OUT} short-circuit protection

The IXD3248A controller assumes that the output voltage V_{OUT} is shorted to GND if the FB pin voltage is less than 0.5 of the reference voltage and currents through high/low side transistors of the N-channel MOSFET Driver exceed limits. In this case, the IXD3248A controller turns off the High side and Low side driver transistors immediately, and forces the L_X pin to the ground to discharge load capacitor C_L, latching it in this state. However, the internal circuitries of the IC continue to operate.

To restart controller's operation after this condition, either EN pin should be toggled H – L – H, or V_{IN} pin voltage should be set below UVLO to resume operations from soft start.

LX short-circuit protection

If the LX pin shorted to GND when the High side driver transistor is on, it activates the **High side driver current limiting**, which turns High side transistor off and Low side transistor on. If Low side transistor current is low and does not activate **Low side driver current limiting,** an L_X short-circuit condition is detected, and both Low and High side transistors are turned off and latched in this state.

To restart the controller's operation after this condition, either the EN pin should be toggled H – L – H, or the V_{IN} pin voltage should be set below UVLO to resume operations from soft start.

V_{OUT} over-voltage protection

V_{OUT} over-voltage protection activates when V_{OUT} overshoot occurs due to fast load changing from a heavy to a light one, and the FB voltage rises to 0.9 V or more. In this case, the High side driver transistor turns off immediately and the Low side transistor turns on. When the FB voltage falls to 0.8V or less, normal operation resumes at the next clock cycle.

C_L high-speed discharge function

When the IC enters standby mode due either EN pin set low, or activated protection, the output capacitor C_L discharges at high speed by the internal switch, connected between L_X and GND. This prevent from load malfunction due to C_L charge remained after the IC stops.

The C_L discharge time can be calculated from the equations shown below. Note that equations vary depending on the V_{OUT} voltage.

1) Output voltage 1V ≤ V_{OUT} ≤ 4 V

In this case, load capacitance and discharge circuitry resistance, shown in the Electrical Operating Characteristic table, determine discharge time as

$$t = -\tau \ln \frac{V}{V_{OUT}}, \text{ where:}$$

t – Discharging time, s
τ – Discharge circuitry time constant $\tau = C_L R_{DCHG}$, s
C_L – Load capacitance, F
R_{DCHG} – discharge circuitry resistance shown in Electrical Operating Characteristic table, Ω
V – Voltage remaining on C_L capacitor after discharge, V

2) Output voltage 4.1V ≤ V_{OUT} ≤ 12V

In this case, discharge time is determined by constant current until V_{OUT} = 4 V, and by load capacitance and discharge circuitry resistance, shown in Electrical Operating Characteristic table, after V_{OUT} < 4 V.

$$t = \frac{C_L \times (V_{OUT} - 4)}{I_{DCHG}} - \tau \ln \frac{V}{4} , \text{ where}$$

t – Discharging time, s
τ – Discharge circuitry time constant $\tau = C_L R_{DCHG}$, s
C_L – Load capacitance, F
R_{DCHG} – discharge circuitry resistance shown in Electrical Operating Characteristic table, Ω
I_{DCHG} - discharge current shown in Electrical Operating Characteristic table, A
V – Voltage remaining on C_L capacitor after discharge, V

TYPICAL APPLICATION CIRCUIT
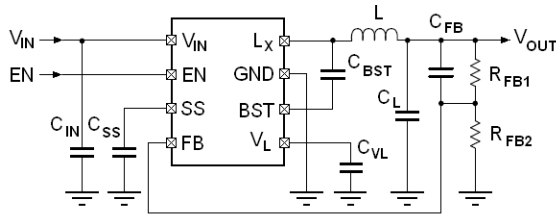
External Components

C_{IN} = 20 µF – two 10 µF 25 V capacitors in parallel

C_L = 44 µF – two 22 µF capacitors in parallel[*1]

C_{BST} = 0.1 µF 10 V

C_{VL} = 0.1 µF 10 V

*1 – C_L rated voltage should be at least 1.5 x V_{OUT}

EXTERNAL COMPONENTS

Recommended Inductors

VALUE	PART NUMBER	MANUFACTURER
10 µH	CLF1004T100N	TDK
6.8 µH	CLF7045T6R8N	TDK
4.5 µH	NR6045T4R5M	Taiyo Yuden
2.2 µH	NR6028T2R2N	Taiyo Yuden

Selecting Inductor

The IXD3248 is optimized for operation at inductor peak current in the range of 0.5 – 1 A.
The inductor peak current value I_{LP} depends on input/output voltage and inductor's value:

$$I_{LP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{0.5 V_{IN} L} + I_{OUT} \text{ , (A), where:}$$

V_{IN} – input voltage, V
V_{OUT} – output voltage, V
L – inductance, µH
I_{OUT} – output current, A

Examples of recommended inductor values are in the table below.

V_{IN}, V	V_{OUT}, V	L, µH	I_{LP}, A
5.0	1.0	2.2	0.73
5.0	2.5	3.3	0.78
12.0	3.3	6.8	0.7
12.0	5.0	6.8	0.86
18.0	5.0	10.0	0.72
18.0	12.0	10.0	0.80

Inductor value also determines the minimum output voltage as a function of minimum duty cycle: $V_{OUT} = V_{IN} \times D_{MIN}$. Minimum duty cycle vs. inductor value is shown in the table below.

L, µH	D_{MIN}
2.2	18
3.3	20
4.7	21
6.8	21
10	22

V_{OUT} Setting

The 0.8V reference voltage allows setting the output voltage in the range of 1.0 V to 12 V by external resistive divider. Values of resistors R_{FB1} and R_{FB2} determine the output voltage as given in the equation below.

$$V_{OUT} = \frac{0.8 \, x \, (R_{FB1} + R_{FB2})}{R_{FB2}}$$

$R_{FB1} + R_{FB2} < 150k\Omega$

Adjust the value of the phase compensation capacitor C_{FB} so that $f_{zfp} = \frac{1}{2\pi C_{FB} R_{FB1}} \sim 7$ kHz to provide stable operations. Adjustments can be in the range from 5 kHz to 50 kHz depending on the value of inductance (L) and load capacitor (C_L).

Example

$R_{FB1} = 47k\Omega$, $R_{FB2} = 15\ k\Omega$, $V_{OUT} = 0.8\ V \times (47k\Omega + 15k\Omega)\ /15k\Omega = 3.3\ V$

$C_{FB} = 470pF$, $fzfb = 1/\ (2\pi \times 470\ pF \times 47\ k\Omega) = 7.2\ kHz$

External soft-start setting

Connect the external capacitor to the SS pin to increase soft start time above value set internally. After the EN pin is set High to start the IDX3248, SS pin starts sourcing current $I_{SS} = 4\ \mu A$ to charge external capacitor. When the SS pin voltage goes above the SS threshold voltage $V_{SSTH} = 1.8$ V, the output voltage reaches about 90% of the set value.

External soft-start time can be calculated by using the following equation:

$$t_{SS} = V_{SSTH} \times C_{SS}\ /\ I_{SS}$$

Example

$C_{SS} = 0.1\mu F$, $t_{SS} = 1.8V \times 0.1\mu F\ /\ 4\mu A \times 1000 = 45\ ms$
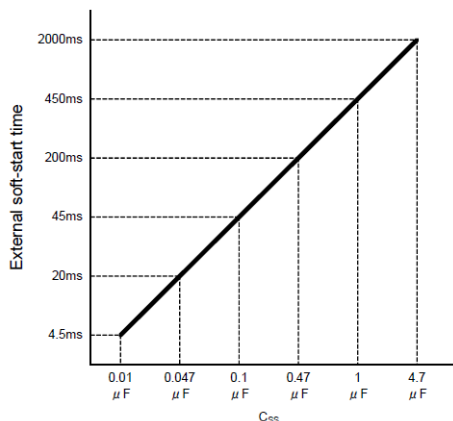
LAYOUT AND USE CONSIDERATIONS

1. Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance. Please, pay special attention to the V_{IN} and GND wiring. Switching noise, which occurs from the GND, may cause the instability of the IC, so, position V_{IN} and V_L capacitors as close to IC as possible.
2. The IXD3248 is designed to work with ceramic output capacitors. We recommend capacitors with X7R or X5R ceramic.
3. This IC monitors peak inductor current using Low/High side current limiting circuits. However, this current depends on the difference between the input and output voltage, as well as the inductor's value. Therefore, in some cases, current limiting may activates too early and cause operation to become unstable, or limit current below maximum value. Pay attention to choose correct inductor value depend on input/output voltage and required load.
4. V_{OUT} voltage drop conveys directly to the FB pin through C_{FB}. When a sharp load fluctuation occurs, the short-circuit protection may activate even at FB pin voltage higher than $0.5V_{REF}$. The IXD3248A controller will latch at this condition; therefore, we recommend use of the IXD3248B controller, if fast fluctuations in load are expected.
5. The VL pin is the output of the internal regulator optimized to supply power for internal IC circuitry. Connect an external capacitor C_{VL} to the V_L pin for stable operation. Do not use the V_L pin to power external circuitry.
6. The IXD3248 may become unstable at input voltage below minimum operating range.

TEST CIRCUITS

Circuit ①
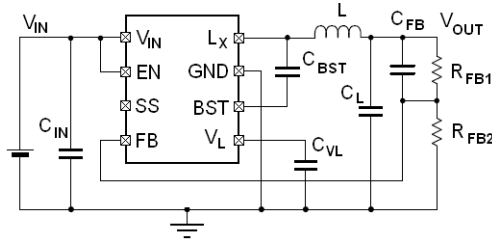
C_{IN} = 20 µF (2 x 10 µF in parallel)
C_L = 44 µF (2 x 22 µF in parallel)
C_{VL} = 0.1 µF, C_{BST} = 0.1 µF

Setup for V_{OUT} = 3.3 V
L = 6.8 µH, R_{FB1} = 47 kΩ, R_{FB2} = 15 kΩ,
C_{FB} = 470 pF

Setup for V_{OUT} = 5.0 V
L = 6.8 µH, R_{FB1} = 43 kΩ, R_{FB2} = 8.2 kΩ, C_{FB} = 470 pF

Circuit ②
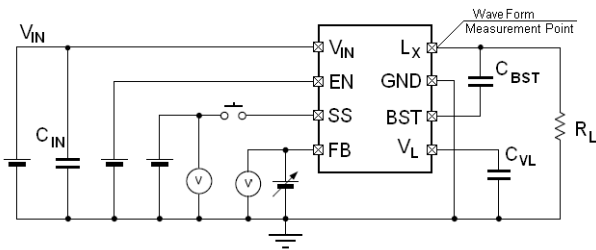
R_L = 300 Ω
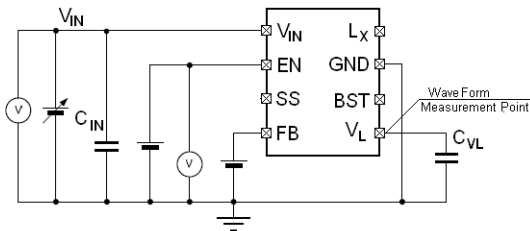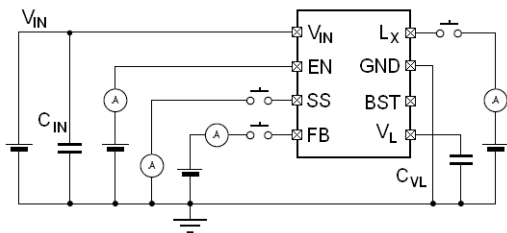
Circuit ③
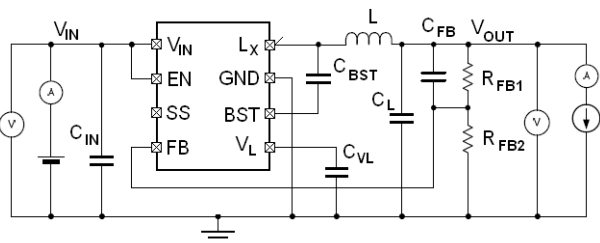
Circuit ④
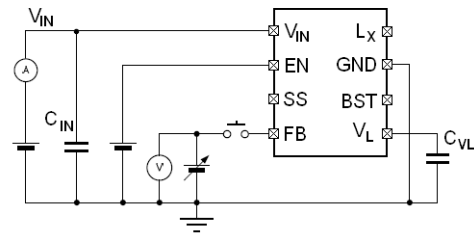
Circuit ⑤
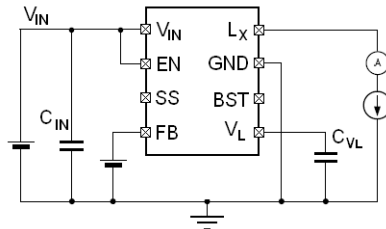
Circuit ⑥

Circuit ⑦

Circuit ⑧
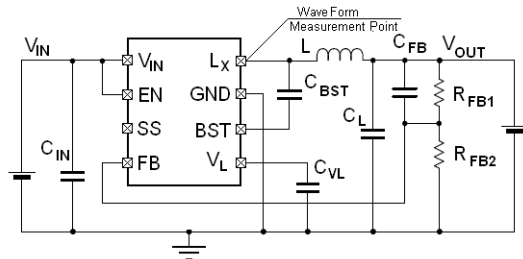
TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output Current

Topr = 25 ^{0}C
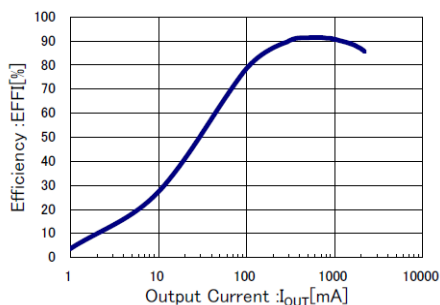
L= 6.8 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 12 V, V_{OUT} = 3.3 V

L= 6.8 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 12 V, V_{OUT} = 5 V

L= 4,5 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 9 V, V_{OUT} = 4 V
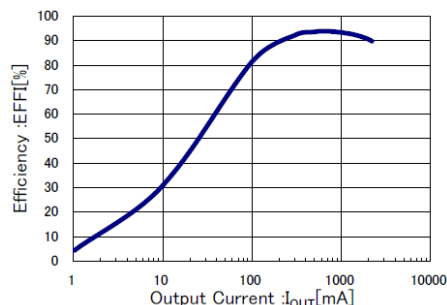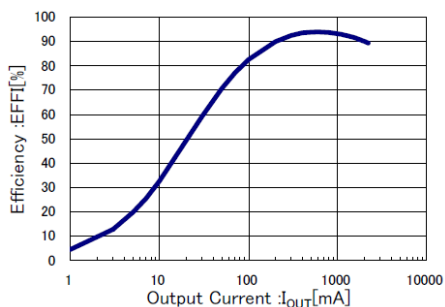
L= 2.2 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 5 V, V_{OUT} = 1 V
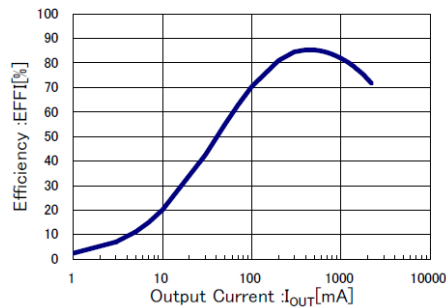
(2) Output Voltage vs. Output Current
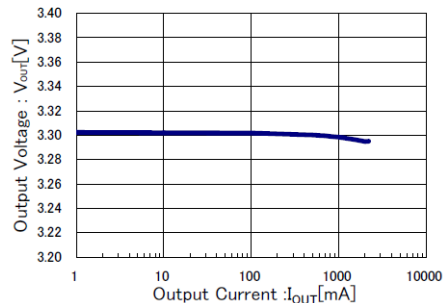
L= 6.8 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 12 V, V_{OUT} = 3.3 V

L= 6.8 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 12 V, V_{OUT} = 5 V

L= 4,5 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 9 V, V_{OUT} = 4 V
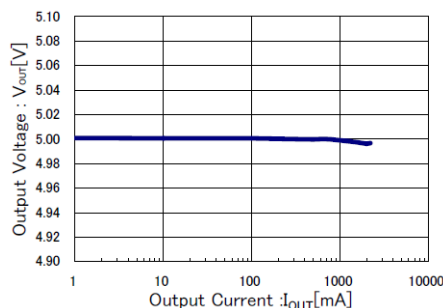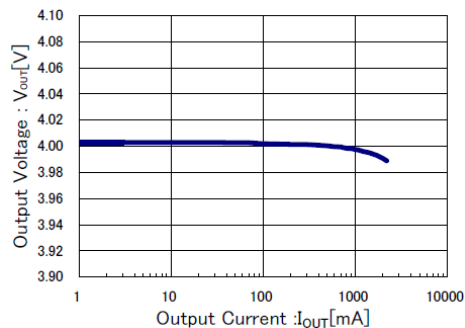
L= 2.2 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 5 V, V_{OUT} = 1 V
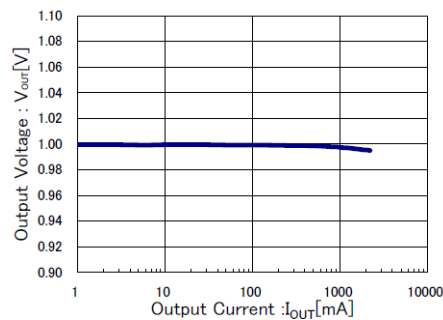
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(3) Ripple Voltage vs. Output Current
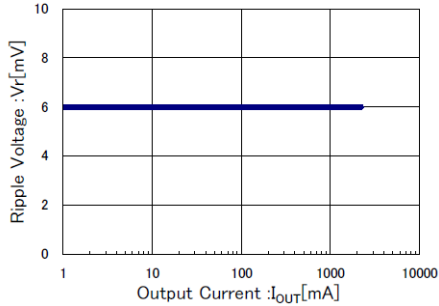
L= 6.8 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 12 V, V_{OUT} = 3.3 V

L= 6.8 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 12 V, V_{OUT} = 5 V

L= 4,5 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 9 V, V_{OUT} = 4 V
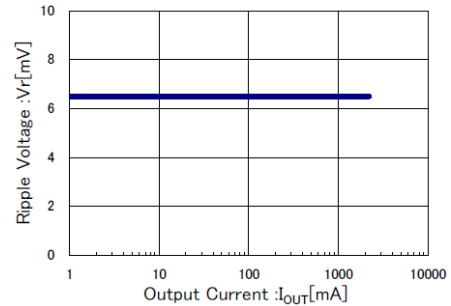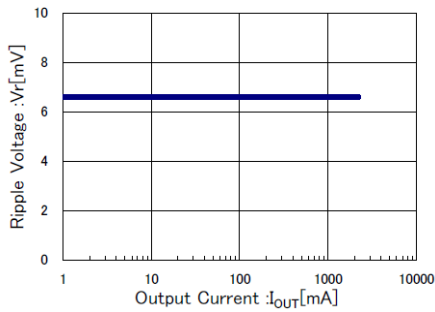
L= 2.2 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 5 V, V_{OUT} = 1 V
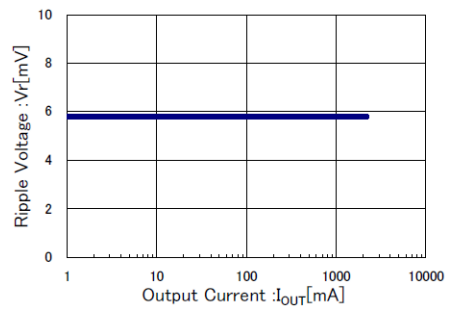
(4) FB Voltage vs. Ambient Temperature
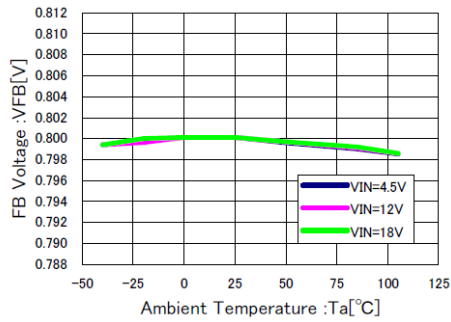
(5) UVLO Voltage vs. Ambient Temperature
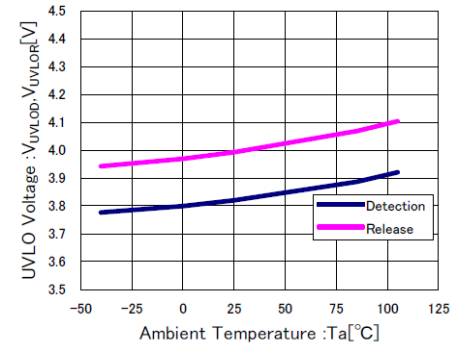
(6) Oscillation Frequency vs. Ambient Temperature
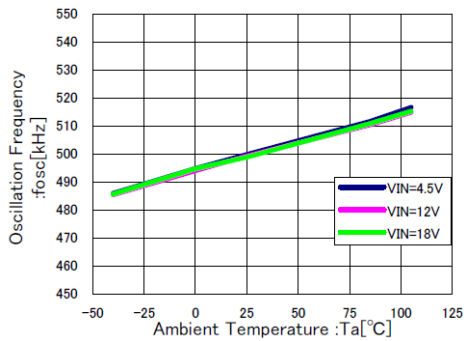
() Supply Current vs. Ambient Temperature
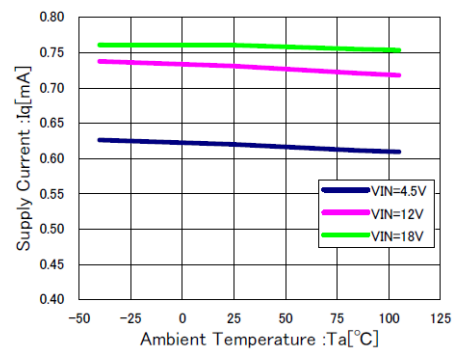
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(8) Standby Current vs. Ambient Temparature
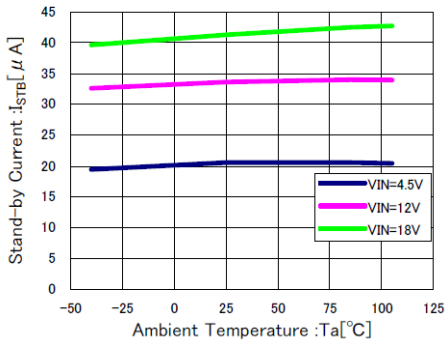
(9) L$_X$ "L" ON Resistance vs. Ambient Temperature
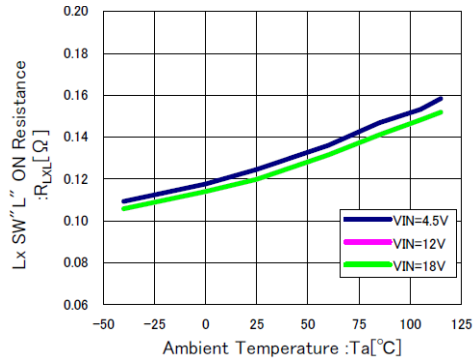
(10) L$_X$ "L" Current vs. Ambient Temperature
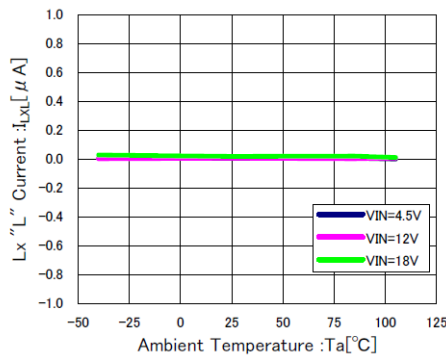
(11) L$_X$ "H" Current vs. Ambient Temperature
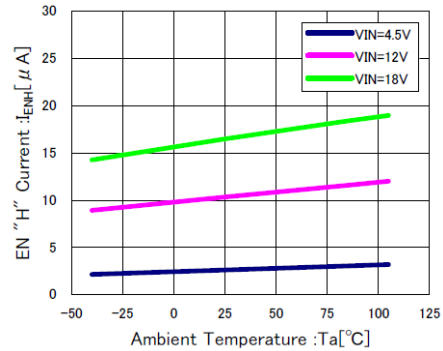
(12) EN "H" Voltage vs. Ambient Temperature
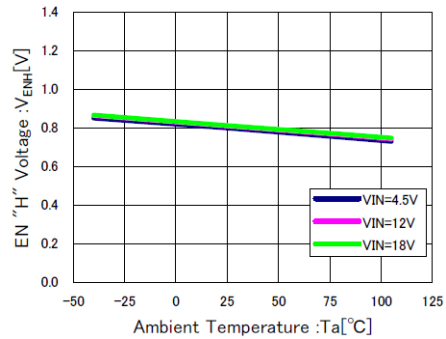
(13) EN "L" Voltage vs. Ambient Temperature
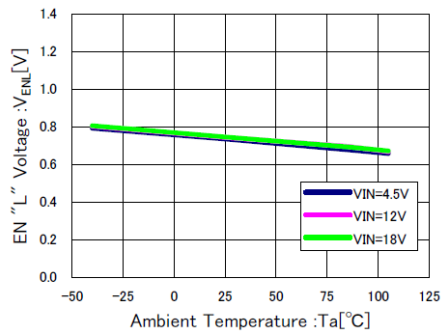
(14) Internal Soft Start Time vs. Ambient Temperature
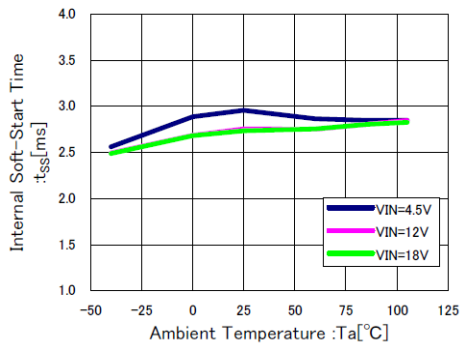
(15) SS Terminal Current vs. Ambient Temperature
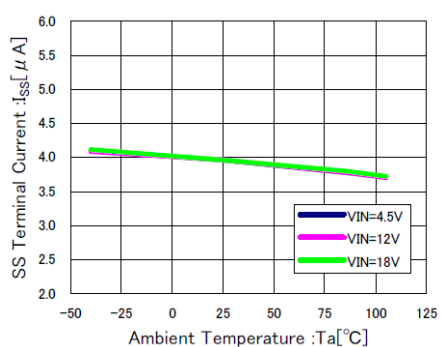
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(16) SS Terminal Voltage vs. Ambient Temperature
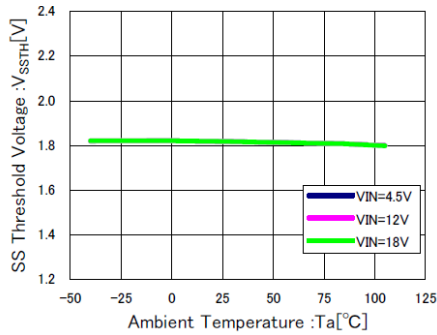
(17) Load Transient Response

I_{LOAD} = 0 mA → 1000 mA
L= 6.8 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 12 V, V_{OUT} = 3.3 V
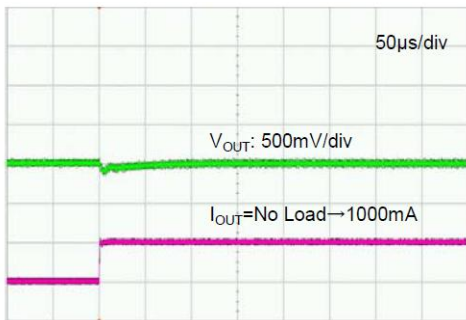
I_{LOAD} = 1000 mA → 0 mA
L= 6.8 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 12 V, V_{OUT} = 3.3 V
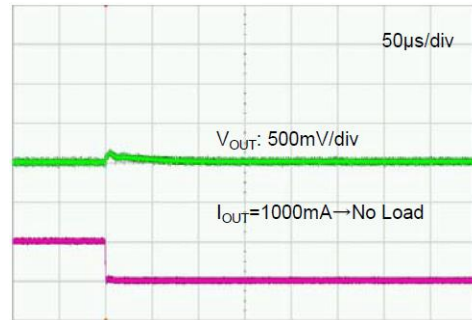
I_{LOAD} = 0 mA → 1000 mA
L= 4,5 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 9 V, V_{OUT} = 4 V

I_{LOAD} = 1000 mA → 0 mA
L= 4,5 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 9 V, V_{OUT} = 4 V
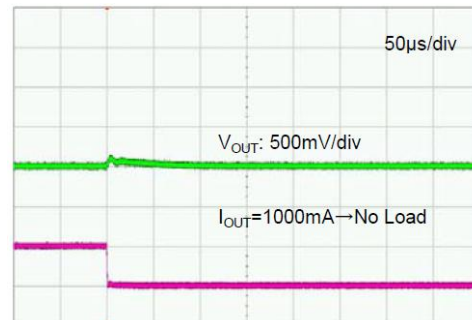
I_{LOAD} = 0 mA → 1000 mA
L= 2.2 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 5 V, V_{OUT} = 1 V

I_{LOAD} = 1000 mA → 0 mA
L= 2.2 µH, C_{IN} =20 µF, C_L= 44 µF, V_{IN} = 5 V, V_{OUT} = 1 V
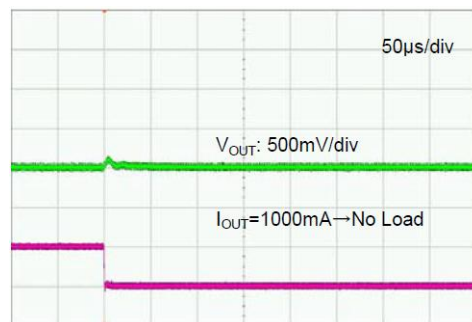
ORDERING INFORMATION

IXD3248①②③④⑤⑥-⑦

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Type of DC/DC Controller	A	Refer to Selection Guide
		B	
②③	Feedback Voltage	08	Feedback Voltage (Fixed) 0.8 V
④	Oscillation Frequency	5	500kHz
⑤⑥-⑦*	Packages (Order Limit)	QR-G	SOP-8FD (1,000/Reel)

(*) The "-G" suffix denotes halogen and antimony free, as well as being fully ROHS compliant.

PRODUCT CLASSIFICATION

Type	CURRENT LIMITER	LATCH AT CURRENT LIMITER	LATCH IF V_{OUT} SHORT	LATCH IF L_X SHORT[2]	ENABLE	UVLO	C_L AUTO DISCHARGE	THERMAL SHUTDOWN
A	Yes	Yes[1]	Yes	Yes	Yes	Yes	Yes	Yes
B	Yes	No	No	Yes	Yes	Yes	Yes	Yes

1) The over-current protection latch is an integral latch type.
2) To prevent an extremely large current from flowing in the event that Lx is short-circuited, both the A & B types have an Lx short protection latch function.
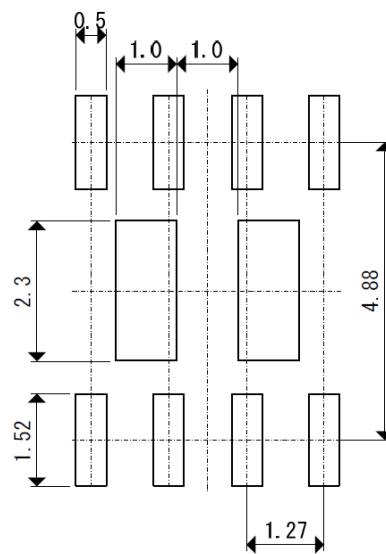
PACKAGE DRAWING AND DIMENSIONS

SOP-8FD (Units: mm)
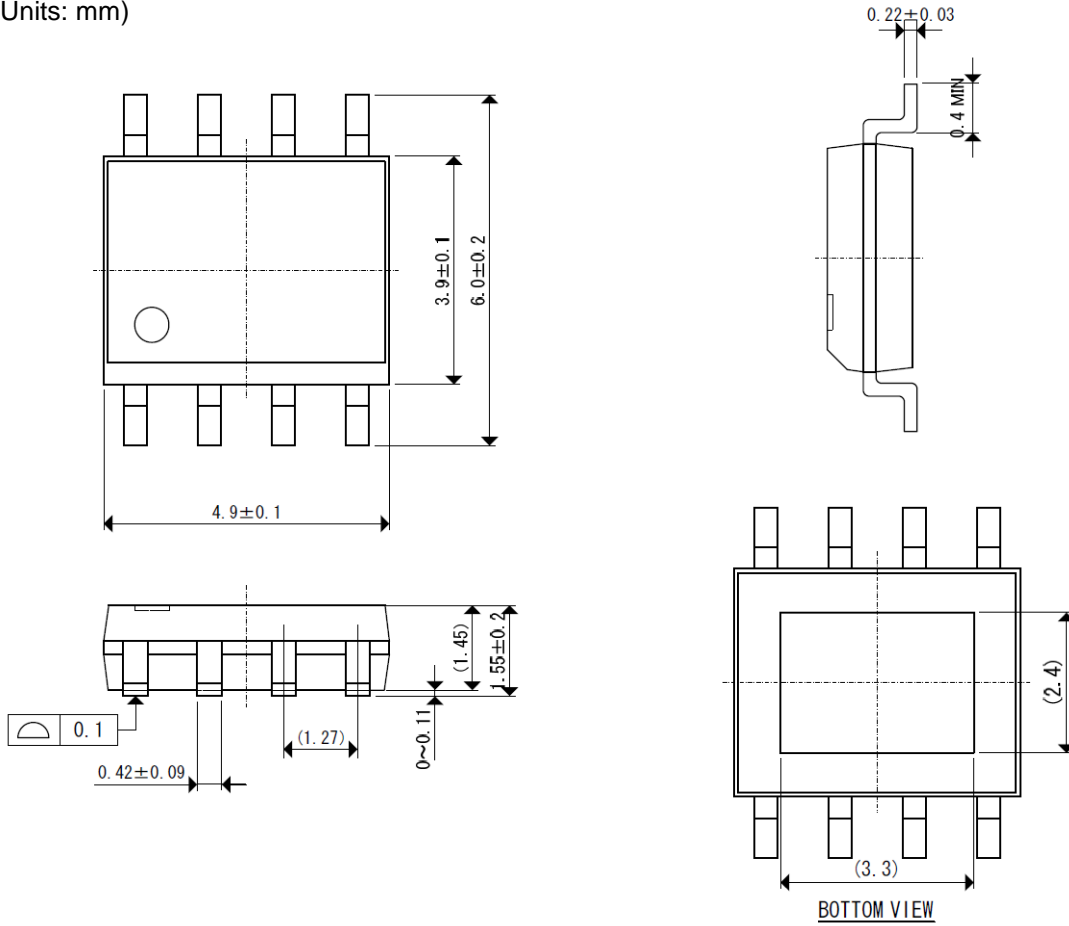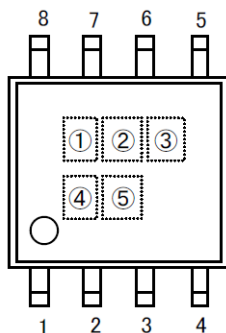
SOP-8FD Reference Pattern Layout (Units: mm)
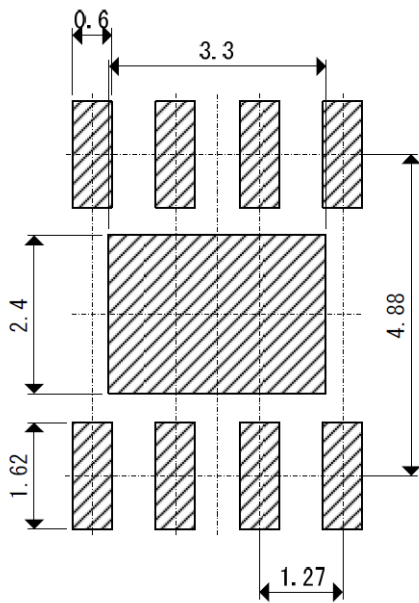
SOP-8FD Referencre Metal Mask Design (Units: mm)

MARKING
SOP-8FD

① represents product series

MARK	PRODUCT SERIES
B	IXD3248xxxxxx-G

② represents product types

MARK	PRODUCT SERIES
A	IXD3248Axxxxx-G
B	IXD3248Bxxxxx-G

③ represents FB voltage and oscillation frequency

MARK	REFERENCE VOLTAGE, V	OSCILLATION FREQUENCY, kHz	PRODUCT SERIES
5	0.8	500	IXD32487x085xx-G

④⑤ represents production lot number

01～09、0A～0Z、11～9Z、A1～A9、AA～AZ、B1～ZZ in order.
(G, I, J, O, Q, and W excluded)

Customer Support

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Warning: DO NOT USE THIS PRODUCT IN LIFE SUPPORT SYSTEMS.