Application Note

Migration from the S3F84YB MCU to the S3F8S7B MCU

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Abstract

This application note highlights the differences resulting from Zilog's transition from the S3F84YB microcontroller to the S3F8S7B version. The migration from the F84YB MCU to the F8S7B MCU is implemented in a manner that facilitates a smooth conversion process. This document provides the information required for a quick transition to the new silicon.

Note: The author assumes the audience has fundamental S3 – S3F84YB knowledge and basic familiarity with Zilog S3 products. To learn more about Zilog's S3 product line, visit zilog.com. For information about the S3F8S7B MCU, refer to the References section.

Device Overview

S3F8S7B single-chip CMOS microcontrollers are fabricated using the highly advanced CMOS process, based on Zilog's newest CPU architecture. The S3F8S7B is a microcontroller with an embedded 64KB Flash ROM. Using a proven modular design approach, Zilog engineers have successfully developed the S3F8S7B MCU by integrating the following peripheral modules with the powerful SAM8 core:

- Nine programmable I/O ports, including eight 8-bit ports, and one 6-bit port, for a total of 70 pins
- Sixteen bit-programmable pins for external interrupts
- One 8-bit basic timer foroscillation stabilization and watchdog functions (system reset)
- Four 8-bit timer/counter
- Two 16-bit timer/counter with selectable operating modes
- Watch timer for real time
- LCD Controller/driver
- A/D converter with 8 selectable input pins
- D/A converter with 1 selectable output pin
- Synchronous SIO modules
- Two asynchronous UART modules
- Pattern generation module
- Available in 80-pin TQFP and 80-pin QFP packages

Features

- CPU
  - SAM88 RC CPU core
- Memory
  - Program Memory (ROM)
    - 64K x 8 bits program memory
    - Internal Flash memory (program memory)
      * Sector size: 128 bytes
      * 10 years data retention
      * Fast programming time: User program and sector erase available
      * Endurance: 10,000 erase/program cycles
      * External serial programming support
      * Expandable OBPTM (on board program) sector
  - Data Memory (RAM)
    - Including LCD display data memory
    - 2,114 x 8 bits data memory
- Instruction Set
  - 78 instructions
  - Idle and stop instructions added for power-down modes
- 70 I/O Pins
  - I/O: 18 pins (Sharing with other signal pins)
  - I/O: 52 pins (Sharing with LCD signal outputs)
- Interrupts
  - 8 interrupt levels and 31 interrupt sources
  - Fast interrupt processing feature
- 8-Bit Basic Timer
  - Watchdog timer function
  - 4 kinds of clock source
- 8-Bit Timer/Counter A
  - Programmable 8-bit internal timer
  - External event counter function
  - PWM and capture function
- 8-Bit Timer/Counter B
  - Programmable 8-bit internal timer
  - Carrier frequency generator

- Two 8-Bit Timer/Counter (C0/C1)
  - Programmable 8-bit internal timer
  - PWM function
- Two 16-Bit Timer/Counter (D0/D1)
  - Programmable 16-bit internal timer
  - External event counter function
  - PWM and capture function
- Watch Timer
  - Interval time: 1.995mS, 0.125S, 0.25S, and 0.5S at 32.768 kHz
  - 0.5/1/2/4 kHz Selectable buzzer output
- LCD Controller/Driver
  - 44 segments and 8 common terminals
  - 1/2, 1/3, 1/4, and 1/8 duty selectable
  - Capacitor or resistor bias selectable
  - Regulator and booster circuit for LCD bias
- Analog to Digital Converter
  - 8-channel analog input
  - 10-bit conversion resolution
  - 25 µs conversion time
- Digital to Analog Converter
  - 1-channel analog output
  - 8-bit conversion resolution (R-2R)
- Two Channels UART
  - Full-duplex serial I/O interface
  - Four programmable operating modes
  - Auto generating parity bit
- 8-bit Serial I/O Interface
  - 8-bit transmit/receive mode
  - 8-bit receive mode
  - LSB-first or MSB-first transmission selectable
  - Internal or external clock source
- Pattern Generation Module
  - Pattern generation module triggered by timer match signal and software
- Low Voltage Reset (LVR)
  - Criteria voltage: 1.9 V, 2.2 V
  - En/Disable by smart option (ROM address: 3FH)

- Two Power-Down Modes
  - Idle: only CPU clock stops
  - Stop: selected system clock and CPU clock stop
- Oscillation Sources
  - Crystal, ceramic, or RC for main clock
  - Main clock frequency: 0.4 MHz to 12.0 MHz
  - 32.768 kHz crystal oscillation circuit for sub clock
- Instruction Execution Times
  - 333 ns at 12.0 MHz fx (minimum)
  - 122.1 s at 32.768 kHz fxt (minimum)
- Operating Voltage Range
  - 1.8 V to 5.5 V at 0.4 to 4.2 MHz
  - 2.2 V to 5.5 V at 0.4 to 12.0 MHz
- Operating Temperature Range
  - -40 C to +85 C
- Package Type
  - 80-QFP-1420C, 80-TQFP-1212
- IVC
  - Internal Voltage Converter for 5 V operations
- Smart Option
  - Low Voltage Reset (LVR) level and enable/disable are at your hardwired option (ROM address 3FH)
  - ISP related option selectable (ROM address 3EH)

Figure 1 shows a block diagram of the the S3F8S7B MCU.

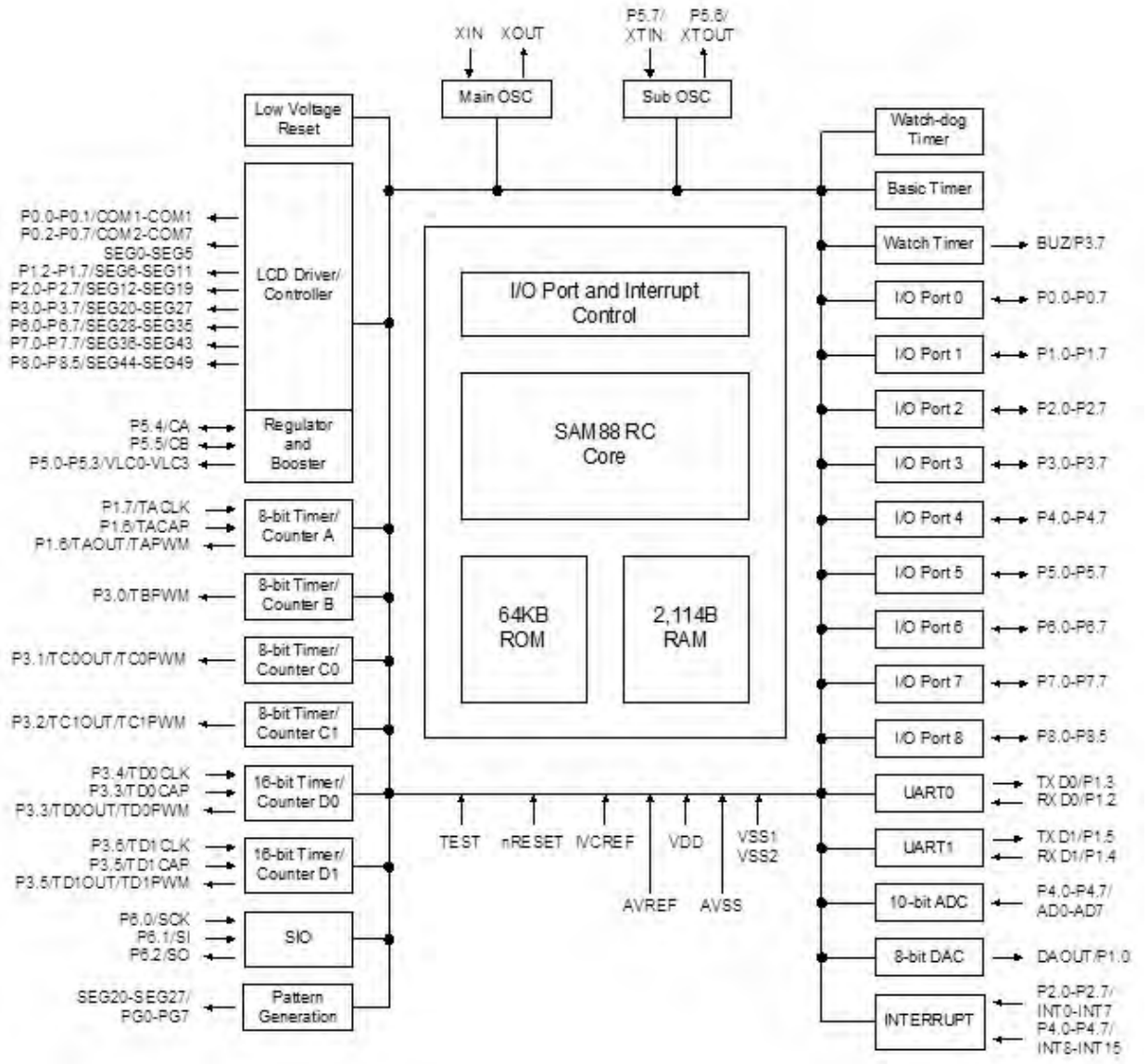

Figure 1. S3F8S7B Block Diagram

Differences Between the S3F84YB and S3F8S7B MCUs

The S3F8S7B MCU has the same pin-out as the S3F84YB MCU, with electrical improvements to the ADC and an enhanced performance in comparison to the S3F84YB microcontroller. The differences are shown in Figures 2 through 5.

Figures 2 and 3 show key differences in the Smart Option and the LVR Electrical Characteristics.

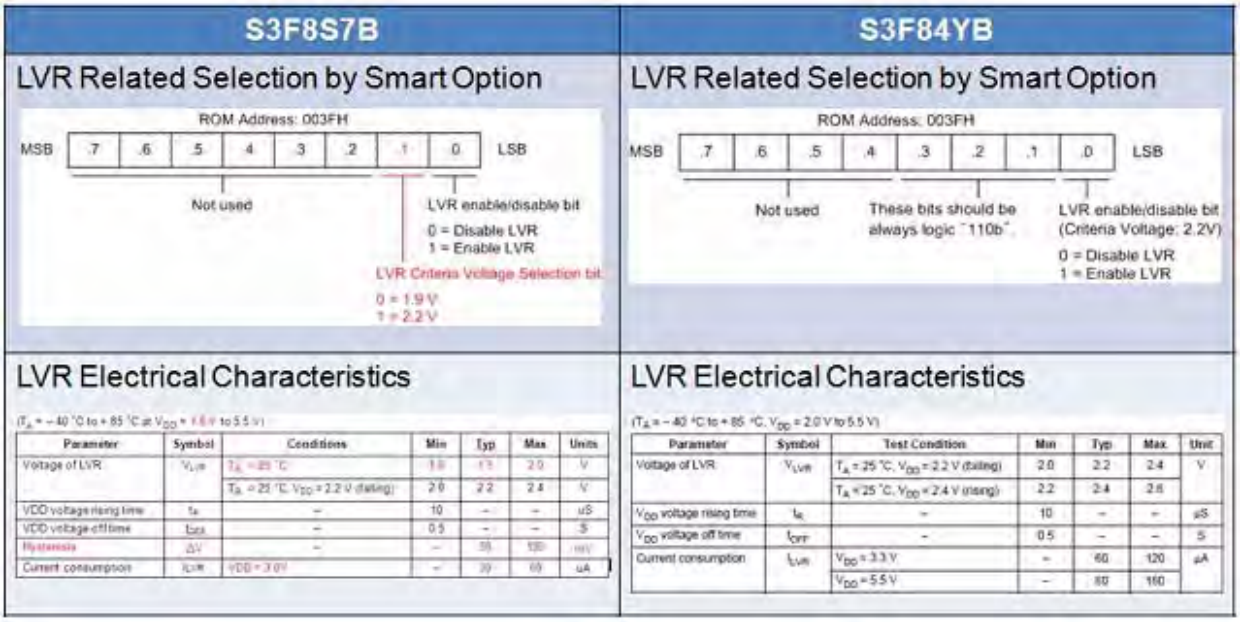

Figure 2. Differences in the Smart Option and LVR Electrical Characteristics

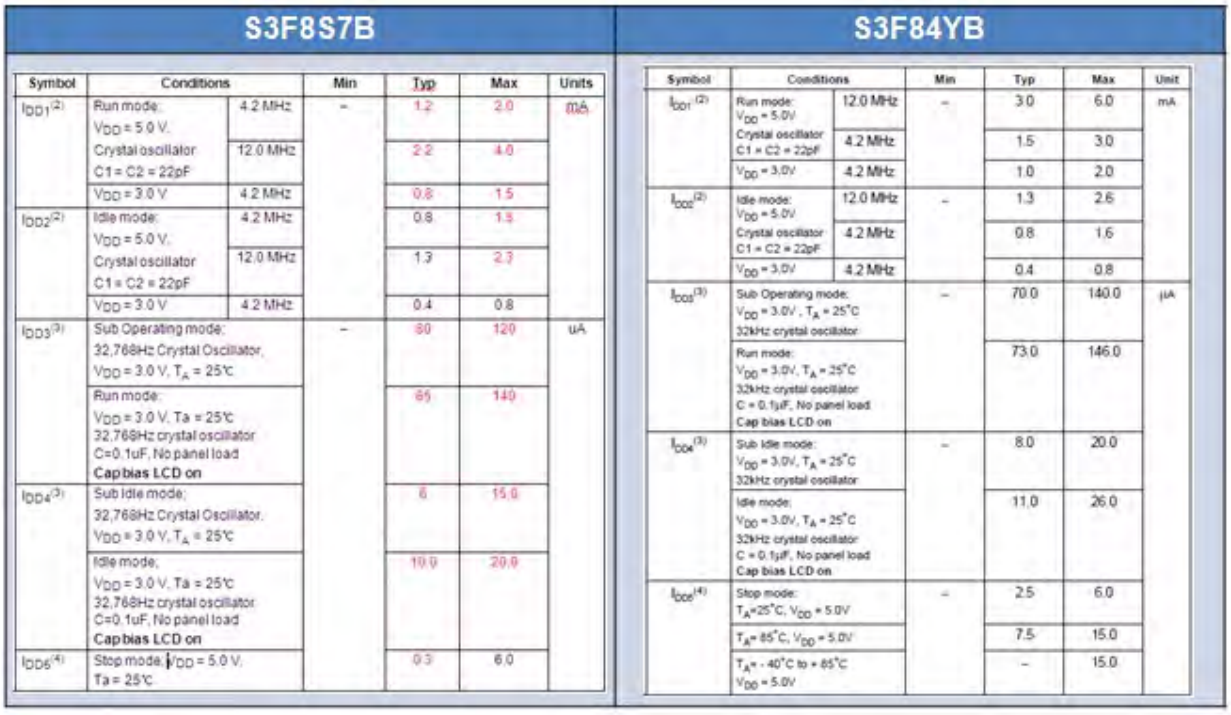

Figure 3. Differences in the LVR Electrical Characteristics

Figure 4 shows the differences in the P4.1/INT9/AD1 and P4.0/INT8/AD0 configuration bits.

S3F8S7B	S3F84YB
P4.1/INT9/AD1 Configuration Bits **P4CONL .3 .2** 0 0 Schmitt trigger input mode 0 1 Schmitt trigger input mode; pull-up 1 0 Alternative function (AD1) 1 1 Push-pull output mode **P4.0/INT8/AD0 Configuration Bits** **P4CONL .1 .0** 0 0 Schmitt trigger input mode 0 1 Schmitt trigger input mode; pull-up 1 0 Alternative function (AD0) 1 1 Push-pull output mode	**P4.1/INT9/AD1 and P4.0/INT8/AD0 Configuration Bits** **P4CONL .3 .2 .1 .0** 0 0 0 0 Schmitt trigger input mode 0 1 0 1 Schmitt trigger input mode; pull-up 1 0 1 0 Alternative function (AD1 and AD0) 1 1 1 1 Push-pull output mode

Figure 4. Differences in the P4.1/INT9/AD1 and P4.0/INT8/AD0 Configuration Bits

Figure 5 shows the differences in the ADCON Bit 3 configuration bit.

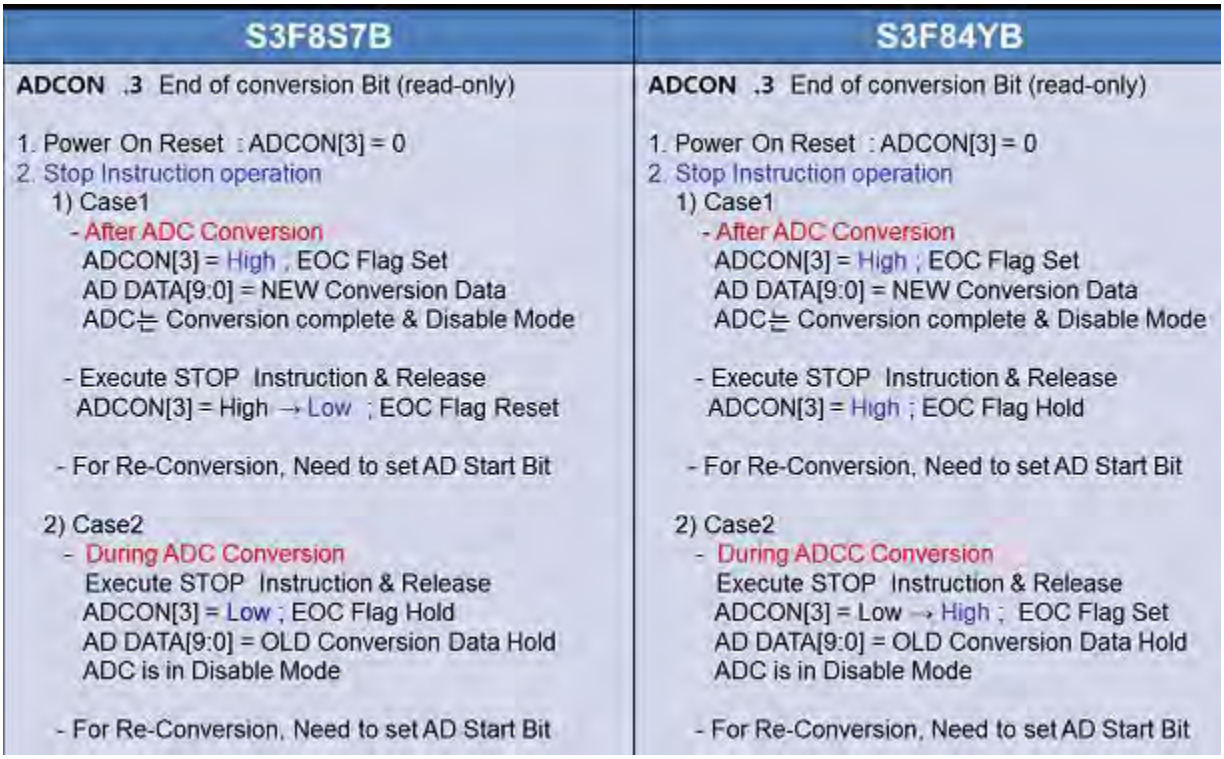

Figure 5. Differences in the ADCON Bit3 Configuration Bit

Summary

Knowledge of the differences between the S3F84YB and S3F8S7B microcontrollers will enable a quick and straightforward migration process. The enhancements from the S3F84YB LVR Electrical Characteristics to the S3F8S7B LVR Electrical Characteristics are expected to benefit the users' applications.

References

The following document is associated with the S3F8S7B MCU:

- S3F8S7B Product Specification (PS0325)

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