

Application Note

Migration from the S3F84YB MCU to the S3F8S7B MCU

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Abstract

Note:

This application note highlights the differences resulting from Zilog's transition from the S3F84YB microcontroller to the S3F8S7B version. The migration from the F84YB MCU to the F8S7B MCU is implemented in a manner that facilitates a smooth conversion process. This document provides the information required for a quick transition to the new silicon.

The author assumes the audience has fundamental S3 – S3F84YB knowledge and basic familiarity with Zilog S3 products. To learn more about Zilog's S3 product line, visit zilog.com. For information about the S3F8S7B MCU, refer to the <u>References</u> section.

Device Overview

S3F8S7B single-chip CMOS microcontrollers are fabricated using the highly advanced CMOS process, based on Zilog's newest CPU architecture. The S3F8S7B is a microcontroller with an embedded 64KB Flash ROM. Using a proven modular design approach, Zilog engineers have successfully developed the S3F8S7B MCU by integrating the following peripheral modules with the powerful SAM8 core:

- Nine programmable I/O ports, including eight 8-bit ports, and one 6-bit port, for a total of 70 pins
- Sixteen bit-programmable pins for external interrupts
- One 8-bit basic timer foroscillation stabilization and watchdog functions (system reset)
- Four 8-bit timer/counter
- Two 16-bit timer/counter with selectable operating modes
- Watch timer for real time
- LCD Controller/driver
- A/D converter with 8 selectable input pins
- D/A converter with 1 selectable output pin
- Synchronous SIO modules
- Two asynchronous UART modules
- Pattern generation module
- Available in 80-pin TQFP and 80-pin QFP packages



Features

- CPU
 - SAM88 RC CPU core
- Memory
 - Program Memory (ROM)
 - 64K x 8 bits program memory
 - Internal Flash memory (program memory)
 - * Sector size: 128 bytes
 - * 10 years data retention
 - * Fast programming time: User program and sector erase available
 - * Endurance: 10,000 erase/program cycles
 - * External serial programming support
 - * Expandable OBPTM (on board program) sector
 - Data Memory (RAM)
 - Including LCD display data memory
 - 2,114 x 8 bits data memory
- Instruction Set
 - 78 instructions
 - Idle and stop instructions added for power-down modes
- 70 I/O Pins
 - I/O: 18 pins (Sharing with other signal pins)
 - I/O: 52 pins (Sharing with LCD signal outputs)
- Interrupts
 - 8 interrupt levels and 31 interrupt sources
 - Fast interrupt processing feature
- 8-Bit Basic Timer
 - Watchdog timer function
 - 4 kinds of clock source
- 8-Bit Timer/Counter A
 - Programmable 8-bit internal timer
 - External event counter function
 - PWM and capture function
- 8-Bit Timer/Counter B
 - Programmable 8-bit internal timer
 - Carrier frequency generator



- Two 8-Bit Timer/Counter (C0/C1)
 - Programmable 8-bit internal timer
 - PWM function
- Two 16-Bit Timer/Counter (D0/D1)
 - Programmable 16-bit internal timer
 - External event counter function
 - PWM and capture function
- Watch Timer
 - Interval time: 1.995mS, 0.125S, 0.25S, and 0.5S at 32.768 kHz
 - 0.5/1/2/4 kHz Selectable buzzer output
- LCD Controller/Driver
 - 44 segments and 8 common terminals
 - 1/2, 1/3, 1/4, and 1/8 duty selectable
 - Capacitor or resistor bias selectable
 - Regulator and booster circuit for LCD bias
- Analog to Digital Converter
 - 8-channel analog input
 - 10-bit conversion resolution
 - 25 μs conversion time
- Digital to Analog Converter
 - 1-channel analog output
 - 8-bit conversion resolution (R-2R)
- Two Channels UART
 - Full-duplex serial I/O interface
 - Four programmable operating modes
 - Auto generating parity bit
- 8-bit Serial I/O Interface
 - 8-bit transmit/receive mode
 - 8-bit receive mode
 - LSB-first or MSB-first transmission selectable
 - Internal or external clock source
- Pattern Generation Module
 - Pattern generation module triggered by timer match signal and software
- Low Voltage Reset (LVR)
 - Criteria voltage: 1.9 V, 2.2 V
 - En/Disable by smart option (ROM address: 3FH)



- Two Power-Down Modes
 - Idle: only CPU clock stops
 - Stop: selected system clock and CPU clock stop
- Oscillation Sources
 - Crystal, ceramic, or RC for main clock
 - Main clock frequency: 0.4 MHz to 12.0 MHz
 - 32.768 kHz crystal oscillation circuit for sub clock
- Instruction Execution Times
 - 333 ns at 12.0 MHz fx (minimum)
 - 122.1 s at 32.768 kHz fxt (minimum)
- Operating Voltage Range
 - 1.8 V to 5.5 V at 0.4 to 4.2 MHz
 - 2.2 V to 5.5 V at 0.4 to 12.0 MHz
- Operating Temperature Range
 - -40 C to +85 C
- Package Type
 80-QFP-1420C, 80-TQFP-1212
- IVC
 - Internal Voltage Converter for 5 V operations
- Smart Option
 - Low Voltage Reset (LVR) level and enable/disable are at your hardwired option (ROM address 3FH)
 - ISP related option selectable (ROM address 3EH)

Figure 1 shows a block diagram of the the S3F8S7B MCU.



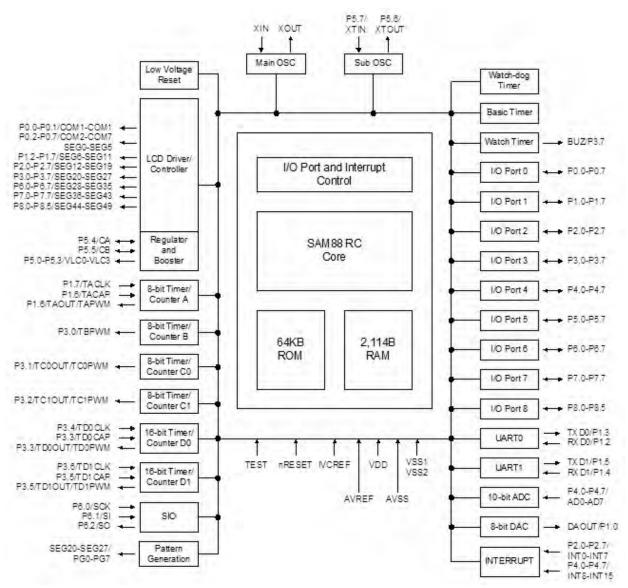


Figure 1. S3F8S7B Block Diagram

Differences Between the S3F84YB and S3F8S7B MCUs

The S3F8S7B MCU has the same pin-out as the S3F84YB MCU, with electrical improvements to the ADC and an enhanced performance in comparison to the S3F84YB microcontroller. The differences are shown in Figures 2 through 5.

Figures 2 and 3 show key differences in the Smart Option and the LVR Electrical Characteristics.



S3F8S7B								S3F84YB											
LVR Relat	ed Se	election by Sm	arto	Opti	on		LVR	Rela	ted	Se	lect	ion b	by S	ma	rt	Opti	on		
	ROM Address: 003FH								ROM Address, 003FH										
MSB 7 .6	7 .6 5 4 3 2 1 0 LSB						MSB	.7	6	5	.4	.3	.2	.1		0	LSB		
	(ADC	used	0 = D	enablei lisable t inable t	LVR	Dit			Not use	d		se bits ays logi			(0	interia 1	ble/disa Voltage ble LVR		
	1.000	Characteristics	2V	Volinge	s Select	tion bit.		Elec				acte	eristi	cs	1	* Enab	le LVR		
LVR Elect	1.000	Characteristics	99 2V		Mas	tion bit.	(T_A=-40	Elec		ove	05.5 VI	acte			1	= Enab	le LVR	Unit	
(T_+ = + 40 °C to + 85 °C #	V00 * 164	Characteristics	97 2V	Volinge Jap			(T_A=-40	i +C to + 85 rameter	C.V _{DD} = 2 Symb	ev to	75.5 VI Te	st Condit	tion					Unit	
(T _A = +40 °C to + 85 °C # Parameter	V _{DD} + 6.6.4 Symbol	0 = 1 1 = 2 Characteristics	99 27	Iyp	Mas	Units	(T _± = - 40 Pa	i +C to + 85 rameter	C.Vop=2		75.5 VI Te (_ = 25 °C.	st Condit V ₀₀ = 2.2	tion V (failing	M 1 2	hin	Тур	Max		
(T _A = +40 °C to + 85 °C # Parameter	V _{DD} + 6.6.4 Symbol	Characteristics	9V 2V	Lyp (1)	Mas 20	Units V	(T _A = - 40 Pa Voitage o	rameter rameter	C. V _{DD} = 2 Symb		75.5 VI Te	st Condit V ₀₀ = 2.2	tion V (failing	1 2 1 2	hin LQ	Typ 2.2	Max. 2.4	V.	
(T _A = +40 °C to + 85 °C at Paraméter Voltage of LVR	V _{DD} + 1.6.4 Symbol V _L (#	Characteristics	9 V 2 V Min 10 2 0	Isp (3 72	Mas 20 23	Units.	(T _± = - 40 Pa Voitage o	1 4C to + 85 rameter f LVR ge rising time	C. V _{DD} = 2 Symb V _L ur		75.5 VI Te (_ = 25 °C.	st Condit V ₀₀ = 2.2	tion V (failing	1 2 1 2 1	han 10 12	Typ 22 24 -	Max. 24 25	V 15	
(T _a + +40 °C to + 85 °C at Peraméter Voltage of LVR VDD voltage rising time	V ₀₀ + 1.6.4 Symbol V _{1.0} 5.	Characteristics	9 V 2 V 10 10	Iyp (3 72	Mas 20 23	Units.	(T ₁ = - 4) Pa Voitage o V ₀₀ voita	rameter rameter	C. V _{DD} = 2 Symb		75.5 VI Te (_ = 25 °C.	st Condit V ₀₀ = 2.2 V ₀₀ = 2.4 -	tion V (failing	1 2 1 2 1 1 0	hun 10	Typ 22 24	Max. 24 28 -	V.	

Figure 2. Differences in the Smart Option and LVR Electrical Characteristics

		S3F8	S7B						S3F	84YB					
Symbol	Conditio	ns	Min	Typ	Max	Units	Symbol	Conditio	onis	Min	Тур	Max	Unit		
IDD1 ⁽²⁾	Run mode. Voo = 5.0 V.	4.2 MHz	-	1.2	2.0	ma	1001 (Z)	Run mode: V _{DD} = 5.0V	12.0 MHz	1	30	6.0	mA		
	Crystal oscillator	12.0 MHz		2.2	4.0	- 1		Crystal oscillator C1 × C2 + 22pF	4.2 MHz		1.5	3.0	1		
	C1= C2 = 22pF							V _{DD} = 3.0V	4.2 MHz		1.0	2.0	1		
1.1.1	Vpc = 3.0 V	4.2 MHz		8.0	1.5		1 ₀₀₂ (2)	Idle mode: Voo = 5.0V	12.0 MHz	-	1.3	2.6	1		
1002(2)	Idle mode: Vpp = 5.0 V,			0.8	13			Crystal oscillator C1 = C2 = 220F	42 MHz	1.1.1	0.8	1.6	1		
	Crystal oscillator	12/0 MHz		1.3	2.7		1.00	V _{D0} = 3.0V	4.2 MHz		0.4	0.8	1		
	C1 = C2 = 22pF Vpp = 3.0 V	4.2 MHz		0.4	0.8	- 1	J _{DOS} ⁽³⁾	Sub Operating mo		-	70.0	140.0	ĮLA		
1003(3)	Sub Operating mod		-	80	120	uA		V _{DD} = 3.0V , T _A = 32kHz crystał osci							
003-4	32,768Hz Crystal O VDD = 3.0 V, T _A = 2	scillator,						Run mode: V _{D0} = 3.0V, T _A = .			73,0	146.0	1		
	Run mode: Vpp = 3.0 V. Ta = 2	3.0 V. Ta = 25%	1		32kHz crystal osc C = 0.1µF. No par Cap bias LCD on	baol len									
	32.768Hz crystal os C=0.1uF, No panel 1 Capbias LCD on						Ipos ⁽³⁾	Sub idle mode: V _{DD} = 3.0V, T _A = 25°C 32kHz crystal oscillator		2	8.0	20.0			
IDD4 ⁽³⁾	Sub idle mode: 32,768Hz Crystal Oscillator. Vpp = 3.0 V, T _A = 25°C		32,768Hz Crystal Oscillator.			6	15,0			Ide mode: V _{DO} = 3.0V, T _A = 25°C 32NHz crystal oscillator			11,0	26.0	1
19	fdle mode;		10.0	20.0	1 1		C = 0.1;if, No par Cap bias LCD on								
	Vpp = 3.0 V. Ta = 2 32.768Hz crystal os	z crystal oscillator		loos ⁽⁴⁾	Stop mode: T _A =25°C, V _{DD} = 5		4	25	6.0	1					
	C=0.1uF, No panel I Cap bias LCD on	030						TA- 85°C, VDD =			7.5	15.0	1		
DD5 ⁽⁴⁾	Stop mode: VDD = 5 Ta = 25°C	.0 V;		03	6.0	1		T _A = - 40°C to + 85 Voc = 5.0V	i'c		-	15.0	1		

Figure 3. Differences in the LVR Electrical Characteristics



Figure 4 shows the differences in the P4.1/INT9/AD1 and P4.0/INT8/AD0 configuration bits.

	S3F84YB P4.1/INT9/AD1 and P4.0/INT8/AD0 Configuration Bits							
P4.1/INT9//								
P4CONL .3	.2							
0	0	Schmitt trigger input mode	P4CONI		.2	.1	.0	
	1			0	0	0	0	Schmitt trigger input mode
1	0	Alternative function (AD1)						Schmitt trigger input mode;
1	1	Push-pull output mode	pull-up					33
			three with	1	0	1	0	Alternative function (AD1 and
P4.0/INT8/	AD0)	-						
	-		10000	1	1	1	1	Push-pull output mode
P4CONL .1	.0							a server to an a start of a start of the
and the second second second second		Schmitt trigger input mode						
	1							
1		Alternative function (AD0)						
1	1	Push-pull output mode						

Figure 4. Differences in the P4.1/INT9/AD1 and P4.0/INT8/AD0 Configuration Bits



Figure 5 shows the differences in the ADCON Bit 3 configuration bit.

S3F8S7B	S3F84YB
ADCON .3 End of conversion Bit (read-only)	ADCON .3 End of conversion Bit (read-only)
1. Power On Reset : ADCON[3] = 0 2. Stop Instruction operation 1) Case1 - After ADC Conversion ADCON[3] = High : EOC Flag Set AD DATA[9:0] = NEW Conversion Data ADC는 Conversion complete & Disable Mode - Execute STOP Instruction & Release ADCON[3] = High → Low ; EOC Flag Reset	1. Power On Reset : ADCON[3] = 0 2. Stop Instruction operation 1) Case1 - After ADC Conversion ADCON[3] = High ; EOC Flag Set AD DATA[9:0] = NEW Conversion Data ADC는 Conversion complete & Disable Mode - Execute STOP Instruction & Release ADCON[3] = High ; EOC Flag Hold
- For Re-Conversion, Need to set AD Start Bit	- For Re-Conversion, Need to set AD Start Bit
2) Case2 - During ADC Conversion Execute STOP Instruction & Release ADCON[3] = Low ; EOC Flag Hold AD DATA[9:0] = OLD Conversion Data Hold ADC is in Disable Mode	2) Case2 - During ADCC Conversion Execute STOP Instruction & Release ADCON[3] = Low → High ; EOC Flag Set AD DATA[9:0] = OLD Conversion Data Hold ADC is in Disable Mode
- For Re-Conversion, Need to set AD Start Bit	- For Re-Conversion, Need to set AD Start Bit

Figure 5. Differences in the ADCON Bit3 Configuration Bit

Summary

Knowledge of the differences between the S3F84YB and S3F8S7B microcontrollers will enable a quick and straightforward migration process. The enhancements from the S3F84YB LVR Electrical Characteristics to the S3F8S7B LVR Electrical Characteristics are expected to benefit the users' applications.

References

The following document is associated with the S3F8S7B MCU:

• <u>S3F8S7B Product Specification (PS0325)</u>



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