Embedded in Life

An IXYS Company

Z02922 TransPro™ Single-Chip Modem

Transaction Processing Modem Data Pump with an Integrated AFE

Product Specification

PS001103-0711

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Revision History

Each instance in the Revision History table below reflects a change to this document from its previous version. For more details, click the appropriate links in the table.

Date	Revision Level	Description	Page No.
Jul 2011	03	Corrections to pin descriptions in Figure 3.	5
		Deleted references to the LQFP package.	All
Aug 2002	02	Minor updates	n/a
Jul 2001	01	Original issue	n/a

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General Description

Zilog's Z02922 TransPro device is a synchronous single-chip modem solution that enables construction of either a V.22bis modem capable of 2400bps full-duplex, or a 9600bps half- duplex over dial-up lines. The Z02922 is specifically designed for use in embedded modem applications where space, performance, and low power consumption are key requirements.

The Z02922 TransPro includes a Quick Connect handshake option that allows the user to make handshakes in 50 milliseconds or less. This feature is especially useful in transaction processing applications such as credit card terminals and network access controllers, where a small amount of data is transmitted.

Operating over the Public Switched Telephone Network (PSTN), the Z02922 TransPro meets the modem standards for V.29, V.22bis, V.22, V.23, V.21, Bell 212A, and Bell 103.

The Z02922 includes automatic handshakes, and also includes manual control over handshake timings. Manual handshake control allows the user to develop handshakes for specific requirements, such as for some point of sale equipment that includes custom handshakes.

A typical modem application can be created by simply adding a control microprocessor (host), phone line interface, and DTE interface. To see a visual representation of these interfaces, refer to Figure 1 on page 4.

The Z02922 TransPro performs HDLC framing at all speeds. This capability eliminates the requirement for an external Serial Input/Output (SIO) device for Data Terminal Equipment (DTE) in products incorporating error control.

All modulation, demodulation, filtering, A/D and D/A conversion functions for transmit and receive are provided on-chip. Automatic and selectable compromise equalizers are included to optimize performance over a wide range of line types.

The Z02922 device compensates for a wide variety of adverse line conditions by using a combination of fixed link, fixed cable, and adaptive equalizers.

The Z02922 provides comprehensive selectable and programmable tone generation and detection.

All digital I/O signals are TTL-compatible. The parallel interface is compatible with standard 8-bit microprocessors, allowing direct access to eight I/O registers and indirect access to the modem RAM.

The RAM access capability allows the host to retrieve diagnostic data, modem/line status and control data, and set programmable coefficients. The serial interface is used for data transfer. All control and status information is transferred by means of the parallel interface.

The Z02922 device's transmit drivers and receive amplifiers can be connected directly to a Data Access Arrangement (DAA) by means of a transformer. Completing this connection reduces the external circuits to a minimum.

In addition, the Z02922 device offers further system level savings by providing built-in filters for both the Transmitter Analog Output and the Receiver Analog Input, thus eliminating the requirement for external filtering components.

The Z02922 device operates on a single +5VDC power supply. During periods of no traffic, the host can place the modem into SLEEP Mode, reducing power consumption to less than 1 percent of full load power.

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low; or $\overline{B}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions, as noted in the table below.

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Features

Device	Data Pump	AFE	Speed (MHz)
Z02922	16-Bit	Integrated	12.288

- Combined data pump and Analog Front-End (AFE)
- Half-duplex data modem throughput to 9600bps
  - ITU V.29 and V.29 Quick Connect™ 9600bps
  - ITU V.29 and V.29 Quick Connect™ 7200bps
- Full-duplex data modem throughput to 2400bps
  - ITU V.22bis, V.23, V.22, V.21
  - Bell 212A and Bell 103
- FSK (V.23 1200/75bps, V.21/Bell 103 300bps), DPSK (V.22/Bell 212A 1200bps), or QAM encoding (V.22bis 2400bps)

- V.29 Quick Connect handshake performs line turnaround in less than 50 milliseconds
- Automatic handshake plus full manual control over handshake timings
- Scrambler/descrambler functions plus selectable control over internal data pump functions
- Programmable Bi-Quad tone detectors for call-progress tone detection
- Adaptive equalization to compensate for a wide variety of line conditions
- Programmable transmit attenuation and selectable receive threshold
- Fully programmable call-progress detectors, signal quality detectors, tone detectors, tone generators, and transmit signal levels which aid in rapid country qualifications
- Host port allows direct parallel interface to standard 8-bit microprocessors
- HDLC framing at all speeds
- On-chip peripherals
  - Full-Duplex voice band AFE with 12-Bit resolution
  - Synchronous serial interface port
  - Eye pattern interface
- Low power consumption: 50 mA typical
- 44-Pin PLCC package
- Single +5 VDC power supply
- 0°C to +70°C commercial temperature range

Note: International Telecommunications Union (ITU), formerly CCITT.

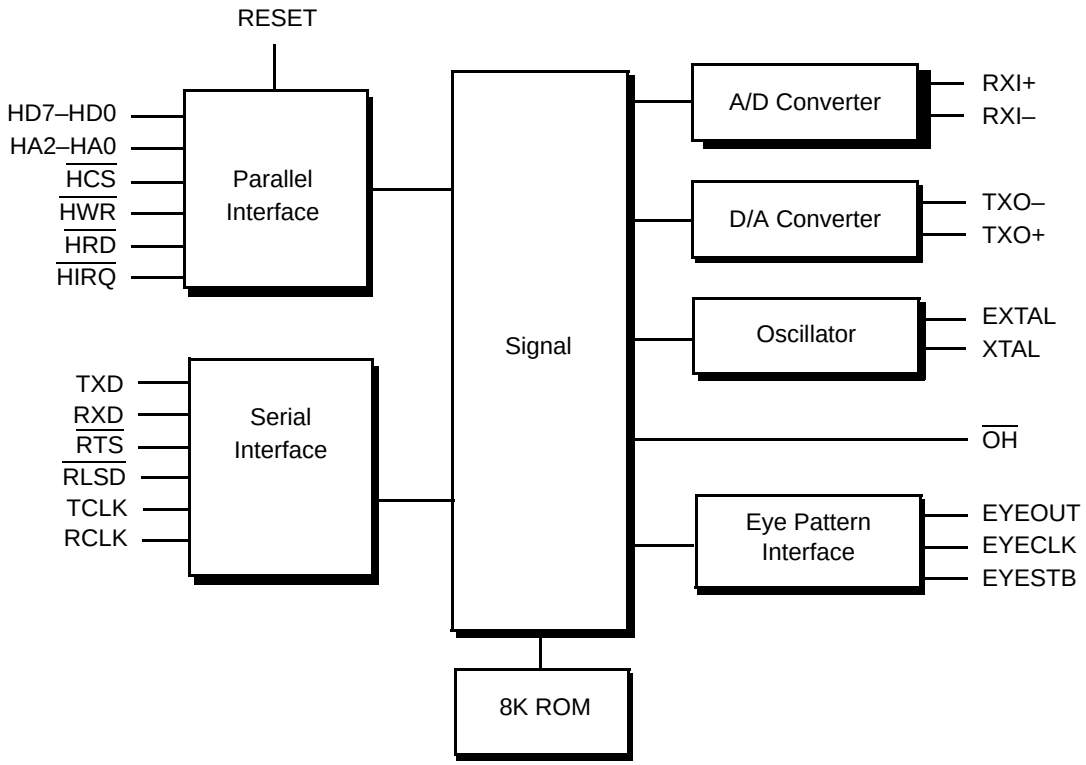


Figure 1. Z02922 Block Diagram

User Information

Zilog's Z02922 TransPro data pump can be selected for either parallel or serial synchronous data transfer under software control. The block diagram in Figure 2 depicts the general modem chip interface. The hardware and software configurations can be customized for a particular modem application. In the diagram, note that the parallel interface allows direct access to 7 I/O registers, indirect access to modem RAM. In addition, this interface is compatible with the Z8, Z80 and Z18X families in addition to other 8-bit microprocessors.

The serial interface is used for data transfer. Controls and status information are transferred via the parallel interface. RAM access capability allows indirect access to diagnostic data, additional status control, and programmable coefficients. The hardware and software interfaces are presented in the subsequent sections.

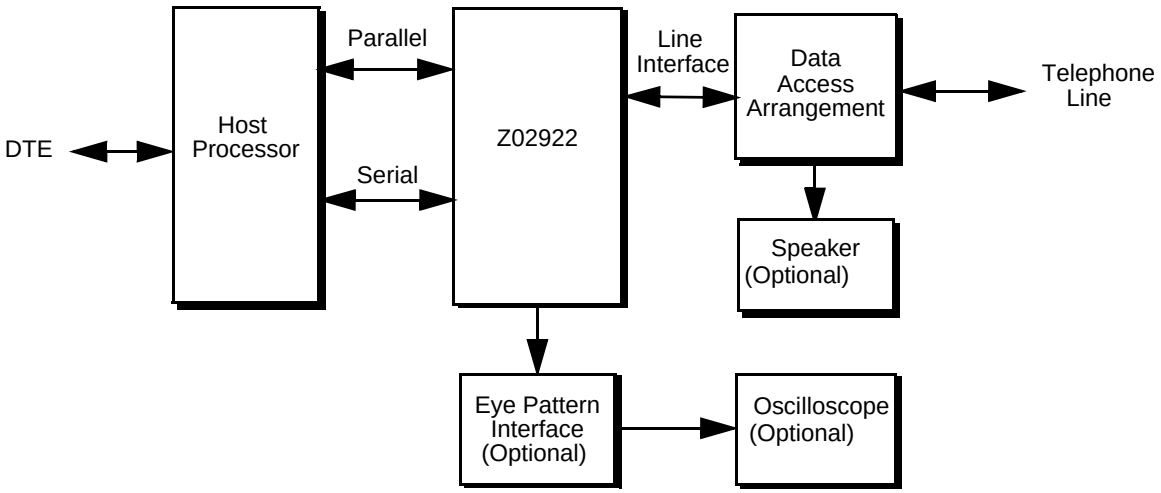


Figure 2. Z02922 System Block Diagram

Pin Description

Figure 3 illustrates the pin assignments for the Z02922 44-Lead PLCC package.

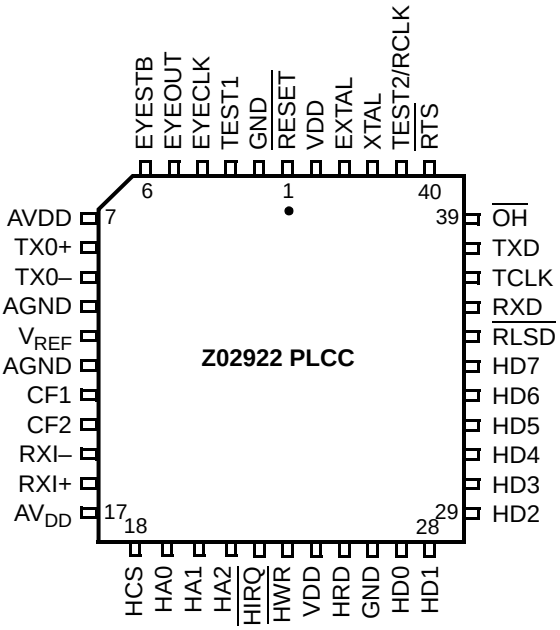


Figure 3. Z02922 44-Lead PLCC Pin Assignments

Pin Signals

For each of the packages shown in Figure 3, Table 29 lists each pin by its number, its signal symbol, and the input/output direction of each pin's signal.

Table 29. Z02922 Pin Assignments

PLCC Pin	Signal	Direction
1	RESET	
2	GND	
3	Test1	Input
4	EYECLK	Output
5	EYEOUT	Output
6	EYESTB	Output
7	AV_{DD}	
8	TXO+	Output
9	TXO-	Output
10	AGND	
11	V_{REF}	Output
12	AGND	
13	CF1	Input
14	CF2	Input
15	RXI–	Input
16	RXI+	Input
17	AVdd	
18	HCS	Input
19	HA0	Input
20	HA1	Input
21	HA2	Input
22	HIRQ	Output
23	HWR	Input
24	V_{DD}	
25	HRD	Input
26	GND	
27	HD0	Input/Output
28	HD1	Input/Output
29	HD2	Input/Output

Table 29. Z02922 Pin Assignments (Continued)

PLCC Pin	Signal	Direction
30	HD3	Input/Output
31	HD4	Input/Output
32	HD5	Input/Output
33	HD6	Input/Output
34	HD7	Input/Output
35	RLSD	Output
36	RxD	Output
37	T_{CLK}	Output
38	TxD	Input
39	OH	Output
40	RTS	Input
41	Test2/R_{CLK}	Input/Output
42	XTAL	Output
43	EXTAL	Input
44	V_{DD}	

Signal Descriptions

This section describes the Z02922 device's signals. Refer to Table 29 to determine package and pins.

HD7–HD0 Host Data Bus (Bidirectional, Active High). HD7–HD0 constitutes an 8-bit bidirectional data bus used for the transfer of control and status information.

HCS Host Chip Select (Input, Active Low). When $\overline{CS}$ is LOW, data transfer between the data pump and the host is enabled. Data transfers to the data pump registers are 8 bits wide.

HWR Host Write Enable Strobe (Input, Active Low). The write enable strobe is an active LOW signal that is used to initiate a write operation to the data pump. During a write operation, data is sent to the data pump by the host via the host data bus.

HRD Host Read Enable Strobe (Input, Active Low). The read enable strobe is an active LOW signal that is used to initiate a read operation from the data pump. During a read operation, data is transferred out of the data pump by the host via the host data bus.

HIRQ Host Interrupt Request (Output, Active Low). The $\overline{HIRQ}$ is an open-drain output that can be tied through an external pull-up resistor to the digital power supply V_{DD}. The $\overline{HIRQ}$ active LOW data pump output can be activated when the host selects this option or

requests by setting the RXIE or TXIE bits in the data pump Host Register. This pin can be connected to the host interrupt request pin to initiate host service.

RESET (Input, Active Low). The $\overline{\text{RESET}}$ signal places the device into its reset state.

HA2–HA0 Host Address (Input, Active High). These three register select lines (pins) are used for addressing the controller-accessible internal registers of the data pump. When $\overline{\text{HCS}}$ is active, the state of these three pins is used as the internal data pump interface register address. HA2 is the most significant bit; HA0 is the least significant bit.

RLSD Receive Line Signal Detect (Output, Active Low). This pin indicates when an input signal has been detected.

RXD Receive Data (Output). The data pump serial receive data is presented by the data pump to the local DTE on the RXD output.

TCLK Transmit Serial Data Clock (Output). The serial data output clock is a synchronous data clock used to transfer serial data between the data pump and the host. The clock frequencies are 2400, 1200, and 300 Hz, corresponding to the supported data bit rates.

TXD Transmit Data (Input). The data pump accepts the serial transmit data from the local DTE on the TXD input when the data pump is configured to the serial transmit data mode. The serial transmit data mode is selected when the TDPM bit (b4) of the RAM control/ data pump Status Register (reg 6) is reset to 0.

OH Off Hook Relay Control (Output, Active Low). This pin is activated to drive a relay which engages the modem with the phone line. (Modem equivalent of picking up the receiver).

RTS Request To Send (Input, Active Low). The logical OR of this pin and the RTSP bit (Reg 4.3), determines the data pump mode of operation. When the result of the logical OR of these two bits is logic 1, then the data pump is in transmit mode at the selected speed, thereby placing the data pump in receive mode. In standby mode, the state of this pin is insignificant.

EYECLK Eye Pattern Clock (Output, Active High). Data is valid at the rising edge of the clock. The EYECLK can be used to clock an external D/A converter shift register for eye pattern display.

EYEOUT Eye Pattern Data (Output, Active High). This pin controls the serial 16-bit eye pattern output data. The first 8 bits is the EYEX data, and the next 8-bits are the EYEY data. This data can be used for display on an oscilloscope X- and Y-axis following D/A conversion.

EYESTB Serial Eye Pattern Strobe (Output, Active High). This signal can be used for loading an external D/A converter.

TXO+ Transmit Differential Analog Output Positive (Analog Output). The TXO+, TXO– is capable of driving a 600-ohm resistive load over a leased line or public switched telephone network via a Data Access Arrangement (DAA). The TXO– and TXO+ can be configured either as a differential or single-ended output driver.

TXO– Transmit Differential Analog Output Negative (Analog Output). The TXO–, TXO+ is capable of driving a 600-ohm resistive load over a leased line or public switched telephone network via a Data Access Arrangement (DAA).

RXI– Receive Differential Analog Input Negative (Analog Input).

RXI+ Receive Differential Analog Input Positive (Analog Input).

TEST1 Test Pin 1 (Input, Active High). This pin is a test pin and must be tied to digital ground.

TEST2/RCLK Test Pin 2, Receive Data Clock (Output, Active High). This pin is a test pin and must be tied to digital ground through a pull-down resistor. The resistor should be LOW enough to ensure this pin floats below 0.8V when the part is in the RESET state. After RESET, this pin becomes the Receive Data Clock Output. The resistor must be high enough to drive the output to 1. This pin is a synchronous data clock used to transfer serial data between the data pump and the host. The clock frequencies are 2400, 1200, and 300 Hz corresponding to the supported data bit rates.

V_{REF} Reference Voltage (Output, Active High. An internally generated reference voltage.

XTAL Crystal (Output, Active High). Crystal oscillator connection. This pin must be left open if an external clock is used instead of a crystal. The data pump chip can be connected to an external crystal circuit consisting of 24.576-MHz (parallel resonant) crystal, a resistor, and two capacitors.

EXTAL External Clock/Crystal (Input, Active High). Crystal oscillator connection. An external clock can be input to the Z02280 on this pin when a crystal is not used. The oscillator input is not a TTL-level (reference DC characteristics).

CF1 and CF2 Integration Capacitor Pins 1 and 2 (Analog Input). Connect an 82 pF capacitor between CF2 and CF1 to complete the internal feedback integration filter for improved analog A/D performance.

GND Digital Ground: 0 Volts.

V_{DD} Digital Power–5 Volts.

AV_{DD} Analog Power–5 Volts.

AGND Analog Ground–0 Volts.

Electrical Characteristics

The data in this section represents all known data prior to qualification and characterization of the Z02922 TransPro™ device, and is therefore subject to change. Additional electrical characteristics may be found in the individual chapters of this document.

Absolute Maximum Ratings

Stresses greater than those listed in Table 30 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, tie unused inputs to one of the supply voltages (V_{DD} or V_{SS}).

Table 30. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	–0.3	+7.0	V
T_{OPR} (com)	Operating Temperature	0	+70	°C
T_{STG}	Storage Temperature	–65	+150	°C

Environmental and Power Requirements

The modem power and environmental requirements of the Z0922 device are indicated in Tables 31 and 32.

Table 31. Modem Power Requirements

Voltage	Current Typical @ 25°C	Current Maximum @ 0°C
+5 V_{DC}, Operating	50mA	<=100mA
+5 V_{DC}, Sleep	25µA	<=125µA

Note: All voltages are ±5% DC and must feature ripple less than 0.1V, peak to peak. If switching supply is used, the frequency ranges may be between 20kHz and 150kHz. No component of the switching frequency should be present outside of the supply greater than 500µV peak.

Table 32. Environmental Requirements

Parameter	Value
Ambient Temperature Under Bias (Commercial Temp Range)	0°C to +70°C
Storage Temperature	–65°C to +150°C
Voltage on any pin to V_{SS}	–0.3V to +7V
Power Dissipation	250 mW
Soldering Temperature 0.5 sec	+230°C

Table 33 specifies suggested values for the crystal under differing capacitance loads.

Table 33. Suggested Crystal Specification ($C_1 = C_2 = 20pF$[1], $C_0 = 2pF$)[2]

Parameter	Value
Temperature Range (Commercial)	0°C to +70°C
Nominal Frequency @ 25°C	24.576MHz
Frequency Tolerance @ 25°C	±20ppm
Temperature Stability @ 0°C to 70°C	±25ppm
Calibration Mode	Parallel Resonant
Shunt Capacitance	4pF max.
Load Capacitance	15pF
Drive Level	1.5mW max.
Aging, per Year Max.	± 5ppm
Oscillation Mode	Fundamental
Series Resistance	25Ω max.
Q	70

Notes:
1. Includes pin parasitics.
2. Suggested reading: IEEE JSSC pp. 222–228, April 1980; IEEE JSSC pp. 744–783, June 1988.

DC Characteristics

The Z02922 device's DC parameters are tested under standard test conditions; characteristics are shown in Table 34. The Z02922 testing device applied active loads which were used to test conditions for I_{OH} and I_{OR}.

All testing was conducted within a standard temperature range of 0°C to +70°C and the Voltage Supply Range:

$+4.5V \leq V_{CC} \leq + 5.5V$

All AC parameters assume a load capacitance of 100pF. Add a 10ns delay for each 50pF increase in load up to a maximum of 150pF for the data bus, and 100pF for the address and control lines.

Table 34. TDC Pin Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Test Conditions
Pin Types I and I/O: Input and Input-Output						
V_{IH}	Input High Voltage	2	–	V_{CC} +0.3	V	
V_{IL}	Input Low Voltage	0	–	0.8	V	
I_L	Input Leakage Current	–10	–	10	mA	GND <V0<V_{DD}
Pin Types O and IO: Output and Input-Output						
V_{OH}	Output High Voltage	2.4	–	–	V	$_{IOH=}$ –200 mA
V_{OL}	Output Low Voltage	0	–	0.4	V	$_{IOI=}$ –2.2 mA
I_{OZ}	Tri-state Leakage Current	–10	–	10	mA	GND<V0<V_{DD}
Pin Types I-PU and I-PD: Input with Internal Pull-Up/Pull-Down Resistor						
V_{IH}	Input High Voltage	2		V_{CC} +0.3	V	
V_{IL}	Input Low Voltage	0		0.8	V	
I_{IL}	Input Current	–10		10	mA	GND <V0<V_{DD}
Pin Type XI: Crystal Input						
V_{IH}	Input High Voltage	V_{DD} x0.8		V_{DD}	V	
V_{IL}	Input Low Voltage	0				
Pin Type O-OD: Output with Open-Drain						
V_{OL}	Output Low Voltage	0	–	0.4		I_{OI}=2.2 mA
I_{OZ}	Tri-state Leakage Current	–10	–	10	mA	GND<V0<V_{DD}
Pin Type XO: Crystal Output						
V_{OH}	Output High Voltage	V_{DD} –1		V_{DD}	V	I_{OH}=1.0 mA
V_{OL}	Output Low Voltage	0		1	V	I_{OI}=–1.0 mA
Pin Type AI: Analog Input						
V_{DC}	Input Bias Offset	V_{REF} –15	V_{REF}	V_{REF} +15	mV	
I_L	Input Current	–100	–	100	mA	
C_{IN}	Input Capacitance	–	10	–	pF	
R_{IN}	Input Resistance	–	20	–	Kohm	
Pin Type AO: Analog Output						
V_O	Analog Output Voltage	V_{REF} –1.163	V_{REF}	V_{REF} +1.163	mV	
V_{OFF}	Output DC Offset	V_{REF} –40	V_{REF}	V_{REF} +40	mV	
R_O	Output Resistance	–	0.8	–	Ohm	

Table 34. TDC Pin Characteristics (Continued)

Parameter	Description	Minimum	Typical	Maximum	Units	Test Conditions
C_O	Output Capacitance	–	10	–	pF	
Z_I	Load Impedance	400	600	Infinite	Ohm	
Pin Type PWR: Power and Ground						
V_{DD}	Digital Supply Voltage	4.75	5	5.25	V	Voltage
GND	Digital Ground	–	–	0	–	
AV_{DD}	Analog Supply Voltage	V_{DD}	V_{DD}	V_{DD}	V	
AGND	Analog Ground	GND	GND	GND	V	
I_{DD1}	Digital Supply Current	–	45	90	mA	Operating
I_{ADD1}	Analog Supply Current	–	5	10	mA	Operating
I_{DD2}	Digital Supply Current	–	20	100	mA	SLEEP Mode
I_{ADD2}	Analog Supply Current	–	5	25	mA	SLEEP Mode

AC Characteristics

Figure 4 illustrates read/write timing for the Z02922 MPU interface; Table 5 lists the microprocessor interface timing parameters.

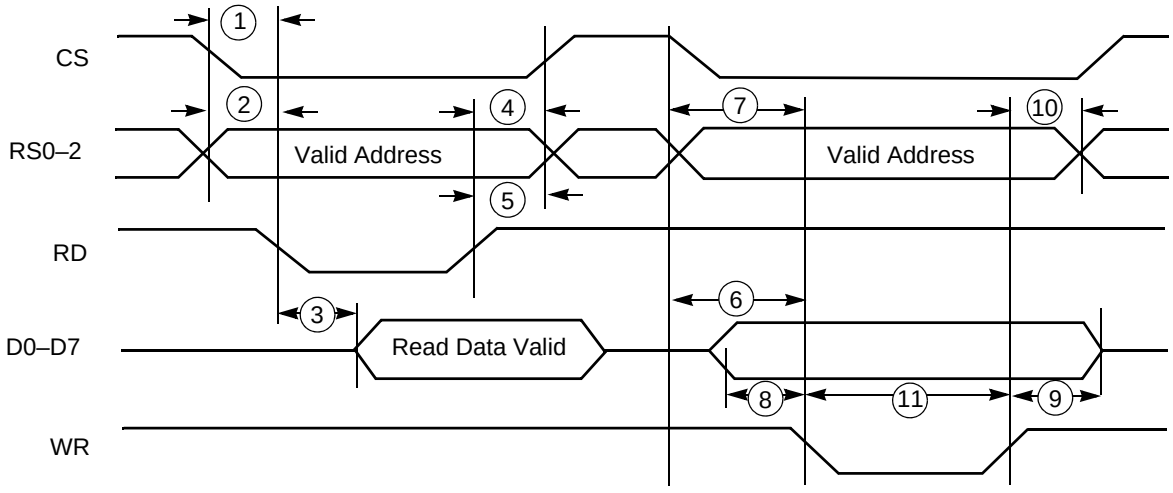


Figure 4. Microprocessor Interface Read/Write Timing

Table 35. Microprocessor Interface Timing

Description	Parameter	Minimum	Typical	Maximum	Units
Read Timing					
HA0–2 and $\overline{HCS}$ to $\overline{HRD}$ Setup Time	1	0	–	–	ns
HA0–2 to $\overline{HRD}$ Setup Time	2	0	–	–	ns
$\overline{HRD}$ to Data Access Time	3	—	25	85	ns
$\overline{HRD}$ Data Hold	4	0	10	–	ns
HA0–2 and $\overline{HCS}$ Hold From $\overline{HRD}$	5	0	–	–	ns
Write Timing					
HA0–2 and $\overline{HCS}$ to $\overline{HWR}$ Setup Time	6	70	–	–	ns
$\overline{HCS}$ to $\overline{HWR}$ Setup Time	7	70	–	–	ns
Data to $\overline{HWR}$ Setup Time	8	0	–	–	ns
$\overline{HWR}$ Data Hold	9	10	–	–	ns
HA0–2 and $\overline{HCS}$ Hold from $\overline{HWR}$	10	10	–	–	ns
$\overline{HWR}$ Pulse Width	11	25	–	–	ns
Reset Timing					
Reset Pulse Width		1.0	–	–	µs
Reset Rise Time			–	100	ns

Figure 5 shows the timing of the serial port; Table 36 lists the serial unterface timing parameters.

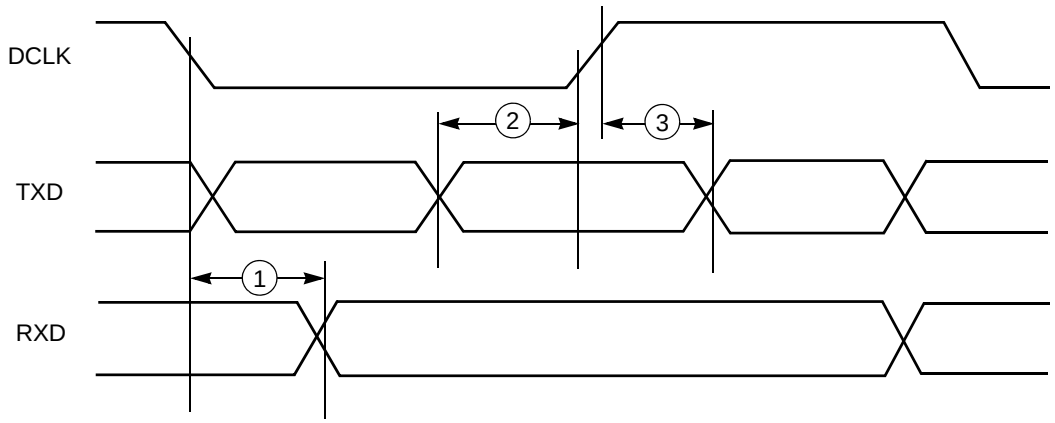


Figure 5. Serial Port Timing Diagram

Table 36. Serial Interface Timing

Description	Parameter	Minimum	Typical	Maximum	Units
RXD Data Valid Delay Time	1	–	12	–	ns
TXD Data Setup Time	2	100	–	–	ns
TXD Data Hold Time	3	100	–	–	ns

Timing Diagrams

Figure 6 shows eye pattern port timing; Table 7 lists analog characteristics for the Z02922 device.

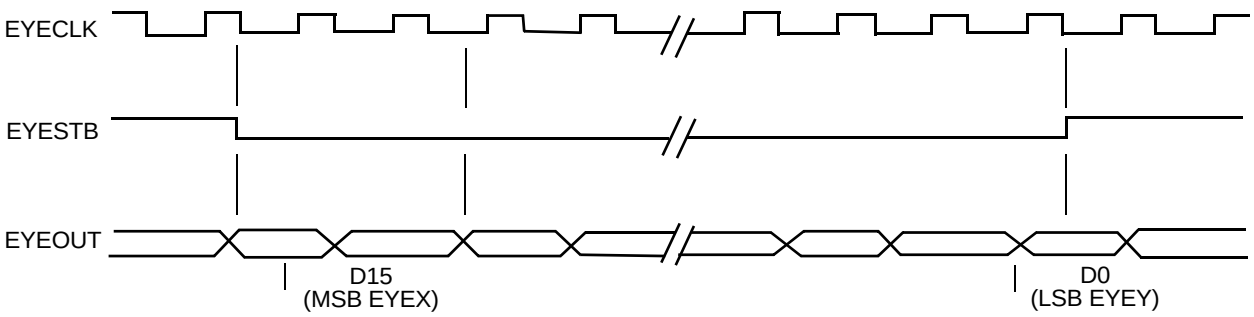


Figure 6. Eye Pattern Port Timing Diagram

Table 37. Analog Characteristics Table

Description	Parameter	Minimum	Typical	Maximum	Units
Input impedance of transformer interface	1	400	1200	–	Ohm
3 dB point of interface	2	21	26.5	32.5	kHz
External integration capacitance Type NPO (COG)	3	73	82	90	pF

Analog Inputs: Type A1

Table 38 lists Type A1 analog inputs for the Z02922 device.

Table 38. Type A1 Analog Inputs

AC Characteristics	Sym	Minimum	Typical	Maximum	Units
Input Impedance (DC to V_{REF})	Z_{IN}	15K	25K	–	Ω
Power Supply Rejection	P_{SRRi}	40	–	–	dB
Input Current	I_i	–80	–	80	µA
Idle Channel Noise (3950 Hz Bandwidth)	I_{CNi}	–	–	–72	dBm
Signal to Distortion	S_{TDi}	30	–	–	dB

Table 39 lists additional analog input characteristics which are provided for information only; these characteristics have not been tested outside of the functional test vectors.

Table 39. Additional Type A1 Characteristics

Characteristics	Sym	Minimum	Typical	Maximum	Units
Input Capacitance	C_{IN}	–	10	–	pF
Input Bias	V_{DCOFF}	–	+2.5	–	V
Analog Input Voltage (peak differential), (23)	V_{PKI}	–2.362	–	+2.362	V
Analog Input Voltage (per RXI+. RXI- pin)	V_{PKIP}	–1.181	–	+1.181	V

Analog Inputs: TYPE A0

Table 40 lists Type A0 analog inputs for the Z02922 device.

Table 40. Type A0 Analog Outputs

AC Characteristics	Sym	Minimum	Typical	Maximum	Units
Power Supply Rejection	P_{SRRO}	40	–	–	dB
Signal to Distortion	S_{TD0}	35	–	–	dB
Idle Channel Noise (3950 Hz Bandwidth)	I_{CNO}	–	–	–72	dBm
Out of Band Noise	N_{qo}				dBm
4–8 kHz	–	–	–20		dBm

Table 40. Type A0 Analog Outputs (Continued)

AC Characteristics	Sym	Minimum	Typical	Maximum	Units
8–12 kHz	–	–	–40		dBm
12kHz and above, in 4kHz bandwidths	–	–	–55		dBm

Table 41 lists additional analog input characteristics which are provided for information only; these characteristics have not been tested outside of the functional test vectors.

Table 41. Additional Type A1 Characteristics

Characteristics	Sym	Minimum	Typical	Maximum	Units
Output Impedance	Z_{OUT}	–	0.80	–	Ω
Output Capacitance	C_{OUT}	–	10	–	pF
Analog Output Voltage (Peak Differential), (24)	V_{PKO}	–2.375	–	+2.375	V
Load Impedance (25)	ZI	400	600	–	–

Hardware Interface Signals

The Z02922 interface consists of a synchronous serial interface port, an 8-bit host microprocessor interface, an Eye Pattern interface, Voice Band AFE, system signals and overhead signals. A functional interconnect diagram of the Z02922 device is shown in Figure 7.

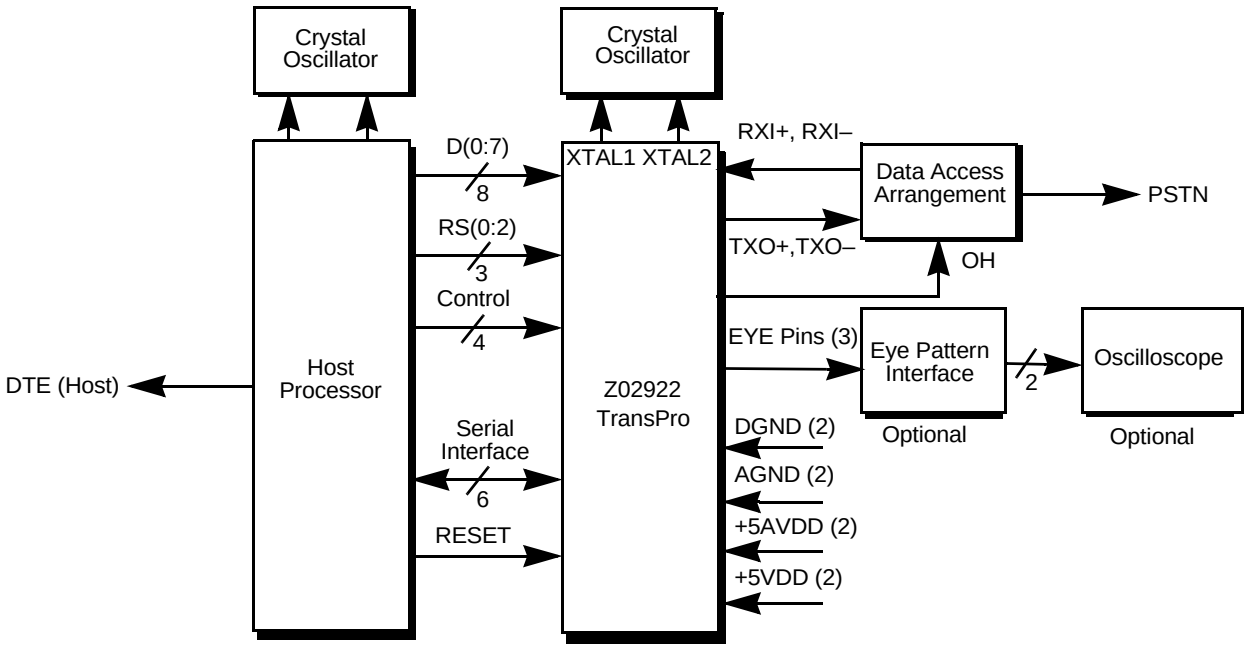


Figure 7. Modem Functional Interconnect Diagram

Synchronous Serial Interface Port

The synchronous serial interface port provides no parallel-to-serial/serial-to-parallel conversion hardware. The synchronous serial interface port consists of 6 signal pins, as indicated in Table 42.

Table 42. Serial Interface Port Signals

Pin	Signal Name
TxD	Transmit Data
RxD	Receive Data
RTS	Request To Send
RLSD	Receive Line Signal Detect
TCLK	Transmit Data Clock
RCLK	Receive Data Clock

Host Port Interface

The host parallel port interface consists of the following 15 signal pins:

- 8-bit bidirectional data bus pins (HD7–HD0)
- 3-bit Address bus (HA2–HA0)
- 4 control lines, which include the Host Read ($\overline{\text{HRD}}$), Host Write ($\overline{\text{HWR}}$), Host Chip Select ($\overline{\text{HCS}}$) and Host Interrupt Request ($\overline{\text{HIRQ}}$)

Multiple interrupt sources are provided in the Z02922 device, each of which can be masked under host control.

The host parallel interface allows the host to access the data pump RAM address and data bits, transmit and receive data, control the RAM and status bits, and read data pump status bits. The host can access eye pattern functions, transmit and receive tones, and access adaptive equalizer coefficients in modem-type applications.

The host parallel interface is compatible with standard 8-bit microprocessors, which include the Z8 and Z80 bus.

Eye Pattern Interface

The eye pattern interface consists of three pins: Eye Pattern Data (EYEOUT), Eye Pattern Clock (EYECLK), and Eye Pattern Strobe (EYESTB). Sixteen bits of data are serially transmitted via EYEOUT, under control of EYESTB and EYECLK. The first byte is the X-coordinate and the second byte is Y-coordinate of the sample. The least significant bit is presented first for both the X and Y coordinates. A schematic of an eye pattern circuit is found in Figure 15 at the end of this specification.

The Eye Pattern Data, EYEOUT, outputs a serial bit stream containing data for display of the eye pattern on an oscilloscope after D/A conversion. Eight bits of the X-axis data and eight bits of the Y-axis are output as a single sixteen bit data stream with the X-axis data first. EYEOUT is synchronous with the rising edge of EYECLK. EYEOUT is valid only while the EYESTB is LOW. Data is shifted out MSB first.

Data on eyeout is shifted out on each rising edge of the 1.536MHz EYECLK. EYEOUT data is valid on the following edge of the Eye Pattern Clock, EYECLK.

The EYEOUT data is valid when the Eye Pattern Strobe, EYESTB, is LOW. EYESTB changes state on the rising edge of EYECLK.

Technical Specifications

This section offers all known specifications for the Z02922 TransPro™ device at the time of the publication of this document.

Configurations and Data Rates

Table 43 provides the selectable options, supported data rate, baud rate, and the modulation method.

Table 43. Selectable Configurations

Configuration[1]	Modulation[2]	Carrier Frequency	Data Rate (bps)	Symbol Rate (baud)	Bits per Symbol	Constellation Points
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	DPSK	1700	7200	2400	3	8
V.22 bis 2400	QAM	1200/2400	2400	600	4	16
V.22 bis 1200	DPSK	1200/2400	1200	600	2	4
V.22 1200	DPSK	1200/2400	1200	600	2	4
V.23 1200/75	FSK	1700/420	1200/75	1200/75	1	—
V.21	FSK	1080/1750	300	300	1	—
Bell 212A	DPSK	1200/2400	1200	600	2	4
Bell 103	FSK	1170/2125	300	300	1	—

Notes:
1. Configuration is selected through the RAM location Configuration Register bits 6–0 (MODE)
2. QAM=Quadrature Amplitude Modulation, FSK=Frequency Shift Keying, DPSK=Dual Phase Shift Keying

Tone Generation and Tone Detection

The Z02922 device provides comprehensive and flexible tone generation and detection, including all tones required to establish a circuit connection and to setup and control a communication session. The tone generation furnishes the DTMF tones for PSTN auto dialing, and the supervisory tones for call establishment. The tone detection provides support for call-progress monitoring. The detector can also be user-programmed to recognize up to 16 tones.

Data Encoding

The data encoding for the Z02922 device meets both ITU–T recommendations and Bell standards.

Transmitted Data Spectrum

The transmitted data spectrum, with compromise equalization disabled, is shaped in the baseband by the finite impulse response (FIR) filter. Table 44 lists the spectrum characteristics.

Table 44. Spectral Shaping

Mode	Carrier Frequency	Spectral Power Shaping Function
V.22	1200	sqrt 75% Raised Cosine at 600 baud
V.22bis	2400	sqrt 75% Raised Cosine at 600 baud

Note: The carrier and the spectral shaping are selected automatically according to the configuration.

Transmit Levels

The transmit output level of the Z02922 device is programmable in 1 dBm decrements from –6 dBm to –43 dBm. With a default value of –10 dBm, the Z02922 device is measured differentially across pins TX0+ and TX0– with a sinusoidal waveform.

Note: To avoid saturation, the T_X level should be set to –6 dBm or lower by the host. If a higher transmit level is required, it can be accomplished using external op amps.

Receiver Levels

The timing recovery circuit can track a ±0.01% (100 ppm) frequency error in the associated transmit timing source with less than 1.0 dB degradation in performance.

Clamping

Received Data (RxD) is clamped to a constant mark whenever $\overline{\text{RLSD}}$ is off.

Carrier Recovery

The recovery circuit can track a ±7 Hz frequency offset in the receiver carrier with less than 1.0 dB degradation in performance.

Parallel Interface Registers

Note: This section refers to *Version 0x42* of the data pump firmware.

The host microprocessor communicates with the Z02922d evice via the parallel microprocessor bus interface. Access is provided to a set of seven 8-bit interface registers, and through these registers to their corresponding Z02922 RAM memory locations. This interface allows the host to request modem status information and receive data, control the configuration, and load data for transmit. Table 45 summarizes the parallel interface register map.

Table 45. Parallel Interface Register Map

Register Name	Register Number	RS2–0 b2b1b0	MS Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0	Access Method
RAM Access LOW	0	000				RAMDL					R/W
RAM Access HIGH	1	001				RAMDH					R/W
RAM Access Address	2	010				RAMAL					W
Parallel Data	3	011				DATAP					R/W
RAM Control & Status	4	100	TXIE	RXIE	RAMIE	TPDM	RTSP	RAMRW	RAMRQ	RAMAH	R/W
Modem Status	5	101	TXI	RXI	RAMI	DPBUSY	Reserved	RTRND	CDET	RES	R
(HDLC)	7	111	0	0	0	0	0	TEND	RXERR	EOF	R/W

Microprocessor Interface Register and Bit Definitions

Reg0, Reg1 RAMDL, RAMDH: Data Pump RAM Data Registers. RAMDL is the least significant byte and RAMDH is the most significant byte. After a data pump RAM read operation has completed, these registers contain the requested data. When a data pump RAM write operation is started, these registers contain the data written to data pump RAM.

Reg2 RAMAL: Data Pump RAM Data Address. When a data pump RAM read or write operation is started, this byte contains the lower 8 bits of the RAM address. Register 4 (RAMAH), described in Table 46, is the high bit of the RAM address.

Reg3 DATAP: Data Pump Parallel Data. This register contains data transferred to or from the remote modem during the parallel modem (see the Reg4 bit description of TPDM in Table 46). At any reset, when Configuration Register bits 6–0 (MODE) = 0 (standby), the data pump places its firmware version number in this register.

Table 46. REG4: RAM Control Register

Bits	7	6	5	4	3	2	1	0
Field	TXIE	RXIE	RAMIE	TPDM	RTSP	RAMRW	RAMRQ	RAMAH

Bit	Description
[7] TXIE	**Transmit Data Interrupt Enable Bit, Parallel Data Mode Only** When set, this bit causes the data pump to generate an interrupt whenever the TXI bit is set.
[6] RXIE	**Receive Data Interrupt Enable Bit, Parallel Data Mode Only** When set, this bit causes the data pump to generate an interrupt whenever the RXI bit is set.
[5] RAMIE	**RAM Interrupt Enable Bit** Setting this bit allows the data pump to interrupt the host when a RAM read/write request has been completed.
[4] TPDM	**Select Parallel Data Mode** Setting this bit selects the parallel data mode. Resetting it selects the serial data mode.
[3] RTSP	**Register Request to Send Bit** An OR instruction is performed on this bit with the hardware RTS signal received by the data pump on the RTS pin. The host uses either RTS or RTSP, set to 1, to inform the data pump the host is transmitting data. To control the data pump using the RTS signal, set RTSP to 0. To control the data pump using RTSP, hold RTS HIGH.
[2] RAMRW	**Data Pump RAM Read/Write Bit** Set this bit to 0 to request a read of the data pump RAM or a 1 to request a write of data pump RAM.
[1] RAMRQ	**Data Pump RAM Access Request Bit** Set this bit to 1 to request a read or write of the data pump RAM. The data pump sets this bit to 0 when the request has been fulfilled.
[0] RAMAH	**RAM Address High Bit** The most significant bit of the data pump RAM address. This bit should be set to 1 when accessing a data pump RAM address that is greater than 255, or set to 0 for any value below 255.

Note: All the bits in this register (REG 4) default to 0 at power-up or when reset sequences are completed.

Table 47 describes the Data Pump Status Register for REG 5. Table 48 describes the REG7:HDLC Register.

Table 47. REG5: Data Pump Status Register

Bits	7	6	5	4	3	2	1	0
Field	TXI	RXI	RAMI	DPBUSY	Reserved	RTRND	CDET	RES

Bit	Description
[7] TXI	**Transmit Interrupt Status** This bit is set when the data pump is in parallel data transfer mode (TPDM is 1) and the data pump has read the DATAP Register. A write to the DATAP Register clears this bit.
[6] RXI	**Receive Interrupt Status** This bit is set when the data pump is in parallel data transfer mode (TPDM is 1) and the data pump has written a new octet to the DATAP Register. A read from the DATAP Register clears this bit.
[5] RAMI	**Data Pump RAM Interrupt Status** This bit is set when the data pump has processed a RAM read/write request.
[4] DPBUSY	**Data Pump Busy** This bit is set whenever the data pump starts transmitting data and RTSP is 1. When the link is to be terminated, setting RTSP to 0 causes this bit to be reset after the data pump has finished transmitting the most recent data in its internal buffers. When this bit has been reset, it is safe to set Configuration Register bits 6–0 (MODE) bit 6–0 (MODE) to standby mode (0) and hang up the telephone, thus terminating the connection. This bit also indicates when digits are being dialed during timed dialing operation. At any reset, or when the host sets Configuration Register bits 6–0 (MODE) bit 6–0 (MODE) to 0 (standby) the data pump sets DPBUSY to 0. This bit is not valid during HDLC operation.
[3]	**Reserved** This bit is reserved and must be programmed to 0.
[2] RTRND	**Retrain Detect, 2400 bps (V.22bis data mode only)** Retrain sequence is detected when this bit is set. The data pump has detected a retrain request sequence from the remote modem.

Note: The RXI bit is set to logic 1 after the reset sequences. All other bits in this register (REG 5) default to 0 at power up or when reset sequences are completed.

Bit	Description (Continued)
[1] CDET	**Carrier Detect** The data pump sets CDET to 1 when it enters any data mode and is ready to transmit data. In V.29 receive, the data pump sets CDET to 1 when it enters V.29 data mode and is ready to receive data. The data pump sets CDET to 0 during retrains (see Reg5, bit 2 RTRND), and when no signal is detected from the remote modem. See locations RLSDOnThresh and RLSDOffThresh for more information. CDET is inverted and reflected on the data pump's $\overline{\text{RLSD}}$ pin. If CDET is 1, $\overline{\text{RLSD}}$ is LOW (asserted). At any reset, or when the host sets Configuration Register bits 6–0 (MODE) bit 6–0 (MODE) to 0 (standby), the data pump sets CDET to 0.
[0] RES	**Data Pump in RESET Mode** This bit is set whenever the data pump is in RESET mode due to a hardware reset or power-on. The data pump sets RES to 0 when it completes reset.

Note: The RXI bit is set to logic 1 after the reset sequences. All other bits in this register (REG 5) default to 0 at power up or when reset sequences are completed.

Reg7 Data Pump Register 7. These bits represent the state of HDLC frames when the data pump is in the HDLC framing mode. These bits are valid only if BUFCTRL bit 7 (HDLC) is 1. The host must refrain from writing Reg7 to avoid changing the values of bit fields set by the data pump. Bits not defined in Table 47 are reserved or not available for use.

The host reads the HDLC Register immediately before DATAP. The two CRC checksum bytes in received HDLC frames are provided to the host.

At any reset, or when the host sets Configuration Register bits 6–0 (MODE) bits 6–0 (MODE) is 0 (standby), the data pump sets TEND to 0, RXERROR to 0, and EOF to 0.

RAMI, RXI, and TXI Interrupts

The three most significant bits in the RAM Control and data pump Status Registers define the interrupt masks for RAMI, RXI, and TXI. The RAMIE, RXIE, and TXIE enable bits in the RAM Control Register have an AND instruction performed by its corresponding interrupt bits in the Data Pump Status Register. The outputs then have an OR instruction performed on them, driving the $\overline{\text{HIRQ}}$ pin and providing an interrupt to the host interrupt. See Figure 8.

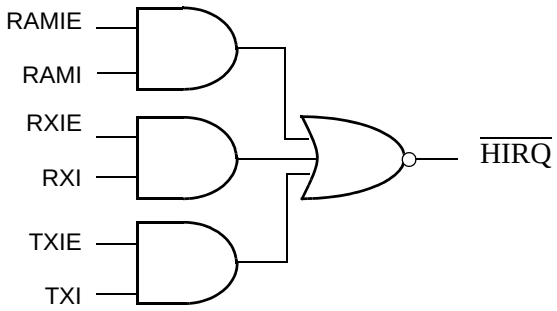


Figure 8. Host Interrupt Circuit Diagram

Interface RAM

The interface RAM is also used by the data pump for normal operations. All writes to the interface RAM must be Read-Modify-Write, where only the bits that must be changed are affected. All undocumented bits are reserved and should be left intact.

Data pump RAM writes take effect at different times, depending on the location being written to. During data modes, writes typically take effect at the end of the next baud period. During other modes of operation, writes take effect in 0.1msec.

Writing Reg4, the RAM Control and Status Register, for example, to set Reg4, bit 6 (TXIE) to 0 in an interrupt handler while waiting for the data pump to set Reg4, bit 1 (RAMRQ) to 0 in the background, may cause unreliable performance. Setting Reg4, bit 1 (RAMRQ) to 1 may cause the data pump to repeat the read/write request if the data pump had just set Reg4, bit 1 (RAMRQ) to 0; however, setting Reg4, bit 1 (RAMRQ) to 0 may abort the RAM read/write request.

Data Pump Interface RAM Access Method

To write to data pump RAM, observe the following brief procedure:

1. Write data to RAMDL and RAMDH.
2. Write the lower 8 bits of the address of the data pump RAM location to Register RAMAL.
3. With one write operation to Register R4, set the High bit of the data pump RAM address in R4, bit 0 (RAMAH), set R4, bit 2 (RAMRW) to 1, and set R4, bit 1 (RAMRQ) to 1.
4. Wait until the data pump sets R4, bit 1 (RAMRQ) to 0.

To read from data pump RAM, observe the following brief procedure:

1. Write the lower 8 bits of the address of the data pump RAM location to Register RAMAL.
2. With one write operation to Register R4, set the High bit of the data pump RAM address in R4, bit 0 (RAMAH), set R4, bit 2 (RAMRW) to 0, and set R4, bit 1 (RAMRQ) to 1.
3. Wait until RAMRQ is reset to 0 by the data pump or until RAMI is 1.
4. Read data from RAMDL and RAMDH.

Reads and writes to data pump RAM may take as much as 105ms to complete.

Modem Data Pump RAM Map

Table 14 summarizes the Modem Data Pump RAM Registers.

Table 48. Modem Data Pump RAM Map

Mnemonic	Address (Hex)	Access Mode	Description
Config	01FF	R/W	Data Pump Configuration
Trnctrl	01FE	R/W	Training Control
Bufctrl	01FD	R/W	Buffer Control
ToneStatus	01FC	R/W	DTMF and Tone Control Status
Dpctrl	01FA	R/W	Data Pump Miscellaneous Controls
MStatus	01F7	R/W	Modem Control and Status
EQMMaxThresh	01F6	R/W	MSE Maximum Threshold
RLSDOffThresh	01F5	R/W	RLSD Off Threshold
RLSDOnThresh	01F4	R/W	RLSD On Threshold
CONN_Mode	01F0	R/W	Connection Speed After Handshake is Complete
DTMFh_lev	01A1	R/W	DTMF High Band Transmit Level
DTMFl_lev	01A0	R/W	DTMF Low Band Transmit Level
ToneGenA	0191	R/W	Tone Generator A
ToneGenB	0196	R/W	Tone Generator B
TxLevel	0185	R/W	Modem Transmit Level
Seq3Count	18E	R/W	Dial Timer Inter-Pulse Count
Seq2Count	18D	R/W	Dial Timer Off Count
Seq1Count	18C	R/W	Dial Timer On Count

Table 48. Modem Data Pump RAM Map (Continued)

Mnemonic	Address (Hex)	Access Mode	Description
BiquadA	0155–015E	R/W	Biquad A Coefficient
BiquadB	015F–0168	R/W	Biquad B Coefficient
DTD0–DTD15	0145–0154	R/W	Tone Detector Coefficients
EQMlev	092	R/W	Eye Quality Monitor Level
BiQuadOffThresh	052	R/W	Biquad Detectors Off Point
BiQuadOnThresh	051	R/W	Biquad Detectors On Point
DTD0Lev–DTD15Lev	026–035	R/W	Tone Detector Levels
DTDThresh	03	R/W	Tone Detector Threshold
DTDStatus	00	R/W	Discrete Tone Detector Status

Interface RAM Definitions

Table 49 describes the modem pump word definitions.

Table 49. Modem Data Pump Word Definitions

Register & Address (hex)	Default Value/Bit	Function and Explanation
CONFIG 01FF	0H	Data Pump Configuration Register
	15	Reserved. This bit must be 0.
	14	**ORG** (Set Originate Mode: All Modes) If ORG is 1, then the modem is in Originate mode. Otherwise, it is in Answer mode. Set ORG before or concurrently with Config, bits 6–0 (MODE), not afterwards.
	13	**ERROR** (Data Pump Error: All Modes) This bit is set to 1 when the data pump detects an internal error condition such as an invalid Config code. The host must reset the data pump.
	12	**ECHOPRTEN** (Echo Protect Tone Enable: V.29) This bit controls the transmission of the Echo Protect Tone (EPT) during a V.29 transmit handshake. EPT is an unmodulated carrier set at –8dBm relative to the transmit level (see Transmit Levels on page 21). If set, the data pump transmits an EPT before transmitting the carrier.
	11	**ECHOPRTLEN** (Echo Protect Tone Length: V.29) This bit controls the length of the EPT tone. 0 (default) selects a 30ms EPT; 1 selects a 185ms EPT.
	10	**MCUCTRL** (Manual Handshake: V.22/V.22bis/B212A) This bit allows the host to control the handshake process in V.22bis. (See Manual Handshake Procedures on page 50 for more information).
	9	**EXTSQLCH** (Extended Squelch: V.29) Set this bit to extend segment 1 (transmitter squelch or silence) in the V.29 training sequence from 20ms to 140ms.
	8	**SRESET** (Soft Reset: All Modes) Set this bit to soft reset the data pump. The data pump sets SRESET to 0 when the software reset completes.
	7	Reserved. This bit must be 0.

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation	
CONFIG 01FF (continued)	6–0	**MODE** (Data Mode Configuration: selects a mode) Selects the data pump operation mode. All modes unlisted below are considered Reserved. The host must read bits 6–0 (MODE), one time after writing it, to allow the data pump enough time to begin operation in the new mode. Setting MODE to 0 (STANDBY) starts the idle mode of operation, not the power-saving SLEEP Mode. The mode is specified by the value assigned to these bits, as follows:	
		Data Mode Specified	
		0	Standby
		1	Transmit tones using both generators simultaneously
		2	Detect tones/BiQuads using all discrete tone detectors and biquad tone detectors simultaneously
		3	Dial
		4	Simultaneous transmission of tones (mode 0X01) and detection of tones (mode 0x02)
		7	SLEEP Mode
		8	V.22bis 2400 bps/1200 bps mode
		9	V.22 1200 bps mode
		B	Bell 212A 1200 bps mode
		10	V.21 300 bps mode
		11	Bell 103 300 bps mode
		13	V.23 1200 bps Tx/75 bps Rx mode
		14	V.23 75 bps Tx/1200 bps Rx mode
		20	V.29 and V.29 Quick Connect 9600 bps Data Mode
		21	V.29 and V.29 Quick Connect 7200 bps Data Mode

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation
TRNCTRL 01FE	0H	**Training Control Register** The data pump sets this location to its default value at any reset and when the host sets Config, bits 6–0 (MODE) to 0 or to any data mode. This RAM location controls the handshake process during a manual training process (see Manual Handshake Procedures on page 50 for an example on the use of this interface). This RAM location has no effect when data mode is entered (Trnctrl is 5 or 6).
	7	**SB1DET** Scrambled Binary 1 Detected (1200 bps or 2400 bps). Debounced through 30 ms.
	6	**S1DET** S1 Detected. Debounced through 27 ms
	5	**USB1DET** Unscrambled Marks Detected (1200 bps)
	4	**SB0DET** Scrambled Binary 0 Detected (1200 bps or 2400 bps)
	3	**V22BIS** Force 16 Way Decisions.
	2–0	**TXCTRL** Transmitter Control. Set TXCTRL to control the output of the data pump, using the table below as a guide. The default frequency for the transmitted tone (TXCTRL is 7) is 2225 Hz. The frequency may be changed after setting these bits by changing ToneGenA appropriately. The tone level is controlled by Modem Transmit Level Register.

Value	V.22/Bell 212A/V.22bis Sequence Transmitted
0	Silence: Squelch Transmitter
1	Transmit Unscrambled Binary 1 at 1200 bps
2	Transmit S1 Signal
3	Transmit Scrambled Binary 1 at 1200 bps
4	Transmit Scrambled Binary 1 at 2400 bps
5	Begin V.22, or Bell212A, 1200 bps Data Mode
6	Begin V.22bis 2400 bps Data Mode
7	Transmit Tone. The default frequency for the transmitted tone is 2225 Hz. The frequency may be changed after setting TXCTRL = 7 by changing the Tone Generator A Register (ToneGenA). The tone level is controlled by Modem Transmit Level Register.

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation		
TRNCTRL 01FE (continued)	0H (cont'd)	2–0	**Value**	**FSK (V.21/ Bell 103/ V.23) Sequence Transmitted**
			0	Silence: Squelch Transmitter
			1	Transmit Marks (binary 1)
			2	Transmit Spaces (binary 0)
			5	Begin FSK Data Mode
			7	Transmit Tone. Set the frequency to be transmitted by changing the Tone Generator A Register (ToneGenA) after setting TXCTRL to 7. The tone level is controlled by the Modem Transmit Level Register.
BUFCTRL 01FD	0H	**Buffer Control Register**		
		15–8	Set these bits to 0 when setting Bufctrl.bit 7 (HDLC) to 1.	
		7	**HDLC (Set HDLC Mode: All Data Modes)** When parallel data transfer mode is selected (TPDM is 1) and HDLC is set, the data pump transfers data using the synchronous HDLC mode. In serial mode (TPDM is 0), this bit has no effect. The host sets bits 8–15 to 0 when it sets this bit to 1.	
		3	**SCRDIS (Scrambler Disable: V.22, V.22bis, Bell 212A,V.29)** Set this bit to disable the transmitter scrambler. This action takes precedence over TRNCTRL/TXCTRL.	
		2	**TXMHLD (Hold Tx Output to Marks: all modes)** Set this bit to force the data pump to transmit only marks to the remote modem, disregarding data received from the host.	
		1	**DSCRDIS (Descrambler Disable: V.22, V.22bis, Bell 212A, V.29)** Set this bit to disable the receiver descrambler.	
		0	**RXMHLD (Hold Rx Output to Marks: all modes)** Set RXMHLD=1 to cause the data pump to transmit only marks to the host, disregarding data received from the remote modem.	
ToneStatus 01FC	080H	Biquad Tone Detector Control and Status, Dial Control The data pump sets this location to its default value at any reset.		
		15	*TONEA* (Tone A Detected). The tone frequency programmed in biquad detector A has been detected if this bit is 1.	

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit		Function and Explanation
ToneStatus 01FC (continued)	080H (cont'd)	14	**TONEB Tone B Detected** The tone frequency programmed in biquad detector B has been detected if this bit is 1.
		13	**Cascade Biquad Tone Detectors A & B** The two 4th order biquad tone detectors can be cascaded to form a single 8th order biquad tone detector if this bit is set by the host. The result of the cascaded biquad tone detector is available in ToneStatus.TONEA.
		7	**TONEDIAL Use DTMF to Dial** This bit causes the data pump to use DTMF tone dialing when in dialing mode (Config, bits 6–0 (MODE) is 3).
		5	**SQRDIS Squarer Disable** Set SQRDIS to 1 to cause the data pump to provide the output of biquad detector A directly to the input of biquad detector B, without first squaring it. SQRDIS is valid only when the biquad tone detectors are cascaded (see ToneStatus, bit 13 (CASCADE).
		4	**TIMEDIAL Timed Dialing** Set TIMEDIAL to 1 to cause the data pump to generate timed DTMF tones or pulse dialing. If TIMEDIAL is 0, continuous dialing occurs.

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation
ToneStatus 01FC (continued)	080H (cont'd)	0–3 **Dial Digit** The DTMF digit to be dialed is set here before Config is set for DTMF transmit. See the table below to determine how to set this parameter. For pulse dialing, only digits 0 through 9 are valid:

Digit	Value
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
*	10
#	11
A	12
B	13
C	14
D	15

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation
DPCTRL 01FA	0H	**Data Pump Miscellaneous Controls** Do not modify this location during automatic handshake or retrain. The data pump sets this location to its default value at any reset.
	15	**TXSQLCH (Squelch Transmitter: All Modes)**
	14	**AGCFRZ (Freeze Autogain Control: V.22/V.22bis/Bell 212A)** Set to 1 to freeze AGC adaptation.
	13	**TXSTRN (Set V.29 Transmit Short Train)** Set to 1 to enable V.29 short train transmitter handshake sequence. The remote receiver must also be set for short train.
	12	**RXSTRN (Set V.29 Receive Short Train)** Set to 1 to enable V.29 short train receiver handshake sequence. The remote transmitter must also be set for short train.
	10–11	**LEQTYPE (Link Equalizer Type)** Set LEQTYPE to 0 for a flat line equalizer, or LEQTYPE to 1 for a 3002 line equalizer.
	9	**GTEN (Guard Tone Enable: V.22/V.22bis/Bell 212A)** This bit controls whether a V.22/V.22bis/Bell 212A link is made with a guard tone or not. If it is set, a guard tone is transmitted along with the carrier. This bit must not be enabled in modes other than V.22, V.22bis, and Bell 212A! This bit must be set prior to selecting the mode in the Configuration Register.
	8	**GTSEL (Guard Tone Select: V.22/V.22bis/Bell212A)** This bit selects the guard tone frequency: 0 for 550Hz, and 1 for 1800Hz. This bit must be set prior to selecting the mode in the Configuration Register.
	4	**EQE (EQMlev > EQMMaxThresh: V.22, V.22bis, V.29, BELL 212A)** The data pump sets EQE to 1 when EQMlev exceeds the threshold set in EQMMaxThresh.
	3	**EQFRZ (Freeze Equalizer: All Modes)** Set to 1 to freeze adaptive equalizer (AEQ) adaptation. AEQ coefficients are lost when a mode change (in Config) occurs.
	2	**TSPACE (Select T-spaced vs. T/2-spaced Equalizer: V.29)** This bit, when set to 1, selects a T-spaced AEQ. When reset to 0, it selects a T/2 spaced AEQ. V.22/V.22bis/Bell 212A modes always use a T/2-spaced equalizer.

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation
MStatus 01F7	0H	**Modem Control and Status**
	11	**RETRAIN (Force a Retrain: V.22bis)** When set, this bit forces a retrain if the data pump has a V.22bis connection. The CDET (Register 5 bit 1) bit is set to 0 when the retrain has begun. The CDET bit is set to 1 when the retrain has been completed. The data pump sets RETRAIN to 0 when retrain begins and when the host sets Configuration Register bits 6–0 (MODE) to any data mode.
	2	**OFFHOOK (Enable Off-Hook Relay)** The data pump sets the OH signal to the inverted value of this bit. For example, when OFFHOOK is 1, the data pump sets OH LOW. When OH is LOW, the off-hook relay should be closed in order for the signal from the telephone line to be presented to the data pump. The data pump sets OFFHOOK to 1 when the host sets Configuration Register bits 6–0 (MODE) bits 6–0 (MODE) to 3 (DIAL), or to any data mode. The data pump sets OFFHOOK to 0 at any reset. Modify OFFHOOK only when Configuration Register bits 6–0 (MODE) bits 6–0 (MODE) to 0 (STANDBY) to avoid interference with the data pump's use of this bit.
EQM MaxThresh 01F6	400H	**EQM Maximum Threshold** The upper acceptable limit for the Eye Quality Monitor (EQM). During V.22, V.22bis or Bell 212A data mode, the EQMlev exceeds EQMMaxThresh, and the data pump sets Data Pump Miscellaneous Controls Register bit 4 (EQE) to 1. The data pump sets this location to its default value at any reset. Changes in value take effect at the end of the next baud period.
RLSDOffThresh 01F5	–48 dBm	**Received Line Signal Detect OFF Threshold**

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation
RLSDOnThresh 01F4	–43dBm	**Received Line Signal Detect ON Threshold** This register represents the upper and lower thresholds of the received telephone line energy. If Modem Status Register bit 1 (CDET) is 1, and the telephone line energy falls below RLSDOffThresh, then the data pump sets Modem Status Register bit 1 (CDET) is 0. If Modem Status Register bit 1 (CDET) is 1 and the telephone line energy rises above RLSDOnThresh then the data pump sets Modem Status Register bit 1 (CDET) to 1. These thresholds stabilize Modem Status Register bit 1 (CDET) by hysteresis when RLSDOffThresh is set to a lower value than RLSDOnThresh. Use the following formula where thresh is specified in dBm and is less or equal to 0. $RLSDval = 10^{(power)/20} \cdot 32767$ The data pump sets this location to its default value at any reset. Changes in value take effect after the next baud period.

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation
CONN_Mode 01F0	—	**Connection Mode Register** This RAM location reports the connection type and speed established after handshake is completed. The values for this location are the same as those for Configuration Register bits 6–0 (MODE):

Value	Data Mode Specified
08	V.22bis 2400bps mode
09	V.22 1200bps mode
0B	Bell 212A 1200bps mode
10	V.21 300bps mode
11	Bell 103 300bps mode
13	V.23 1200bps Tx/75bps Rx mode
14	V.23 75bps Tx/1200bps Rx mode
20	V.29 Quick Connect 9600bps mode
21	V.29 Quick Connect 7200bps mode

DTMFh_lev	01A1	–6dBm	**DTMF Transmit Level — High Band**
DTMFl_lev 01A0		–9dBm	**DTMF Transmit Level — Low Band** These are the transmit levels for the DTMF low band (DTMFl_lev) and DTMF high band (DTMFh_lev) frequencies. The levels are set by the following formula where lev is specified in dBm and less or equal to 0. $DTMFlev = 10^{(lev)/20} \cdot 32767$ Change in value takes effect in 0.1msec. The data pump sets these locations to their default values at any reset.

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)		Default Value/Bit	Function and Explanation
ToneGenA 0191		—	**Tone Generator A**
ToneGenB 0196		—	**Tone Generator B** The data pump has two independent tone generators, each simultaneously generating a pure tone with its own transmit level when Configuration Register bits 6–0 (MODE)=1 (transmit tones). The outputs of the tone generators are mixed together. The generated frequencies are set by writing a coefficient to the Tone Generator A (ToneGenA) or the Tone Generator B (ToneGenB) registers. The coefficient is defined as: where f is the frequency of the tone to be generated. $coeff_x = \frac{2\pi \cdot f}{9600} \cdot 4096$ The transmit levels for tone generators A and B are set in locations the DTMF Low Band Transmit Register (DTMFl_lev) and the DTMF High Band Transmit Level (DTMFh_lev) registers, respectively. See Transmitting Tones on page 42 for more information including a description of setting the tone transmission levels.
TxLevel	0185	–10dBm	**Transmit Power Level** To sets the transmit power level, use the formula where power is specified in dBm and less than or equal to –6. $TxLevel = 10^{(power)/20} \cdot 2048$ Change in value takes effect at the end of the baud period.
Seq3Count 18E		None	**Dial Timer Inter-Pulse Count** See Seq1Count, below.
Seq2Count 18D		95msec	**Dial Timer OFF Count** See Seq1Count, below.
Seq1Count 18C		95msec	**Dial Timer ON Count** Seq1Count, Seq2Count, and Seq3Count are timer counts in units of 1/9600 of a second, for DTMF and pulse dialing. For DTMF dialing, Seq1Count is the length of the digit on-time; and Seq2Count is the length of the digit OFF-time. For pulse dialing, Seq1Count is the length of the break period; Seq2Count is the length of the make period; and Seq3Count is the length of the pause after dialing a digit. The data pump sets these locations to their default values when the host sets Configuration Register bits 6–0 (MODE) is 3 (DIAL).

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation
Biquad A Coefficients 0155–015E **Biquad B Coefficients** 015F–0168	15–0 —	**Biquad A and B Coefficients** These locations program the frequency range for the biquad tone detectors. The coefficients are in the following order: b2, b1, a3, a2, a1, B2, B1, A3, A2, A1. See the Call-Progress Monitoring Using Biquad Tone Detectors section on page 46. for more information.
DTD0–DTD15 0145–0154	15–0	**Tone Detector Coefficients** These locations set the tone detector coefficients for the 16 detectors in the system. The coefficients are set by using the following formula: $coeff_{tone} = \cos\left(\frac{2\pi \cdot f_{tone}}{9600}\right) \cdot 32767$ where (2 pi x ftone/9600) is measured in radians. See the Tone Detectors section on page 43. for more information.
EQMlev 092	15–0	**Eye Quality Monitor (EQM)** This register provides a measure of line quality during V.22, V.22bis, or Bell 212A, while computing a running average of the mean square error (MSE) of the received point and decision point. When EQMlev exceeds EQMMaxThresh, Data Pump Miscellaneous Controls Register bit 4 (Dpctrl.EQE) is set to 1; otherwise, it is set to 0.
BiQuadOffThresh 052	–42 dBm	**Biquad Tone Detectors OFF Point** The data pump sets this location to its default value when Configuration Register bits 6–0 (MODE) is set to 2 by the host. This location can be used to set the off point for the Biquad tone detectors. If the power level is below this value, the detector turns off the detection status bit. Use the following formula to set the threshold where the level is in dBm: $Threshold = 10^{(level)/20} \cdot 32767$ The data pump sets this location to its default value when the host sets Configuration Register bits 6–0 (MODE) to 2 (DETECT TONES).

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation
BiQuadOnThresh 051	–35 dBm	**Biquad Tone Detectors ON Point** The data pump sets this location to its default value when Configuration Register bits 6–0 (MODE) is set to 2 by the host. This location can be used to set the “on” point for the Biquad tone detectors. If the power level is above this value, the detector turns on the detection status bit. Use the following formula to set the threshold where level is in dBm: $$Threshold = 10^{(level)/20} \cdot 32767$$ The data pump sets this location to its default value when the host sets Configuration Register bits 6–0 (MODE) to 2 (DETECT TONES).
DTD0Lev– DTD15Lev 26–35	—	**Discrete Tone Detector Levels** These locations represent the tone detector levels when in the Tone Detect mode (Configuration Register bits 6–0 (MODE) is 02H). These areas may be used by the host to determine which tone is dominant if multiple tones are detected. There is no default in these locations.
DTDThresh 03	–24 dBm	**Discrete Tone Detector Threshold** This location programs the threshold for all discrete tone detectors. Any signal whose signal strength is above this threshold turns on the detection bit for that tone. Any signal below this threshold turns off the detection bit for that tone. This location can be programmed using the following formula: $$Threshold = 10^{(level)/20} \cdot 32767$$ This location must be programmed after Configuration Register bits 6–0 (MODE) is set to detect tone (02H), because the data pump resets this location to its default when Configuration Register bits 6–0 (MODE) is set to tone DETECT mode. See “Tone Detectors” for more information.

Table 49. Modem Data Pump Word Definitions (Continued)

Register & Address (hex)	Default Value/Bit	Function and Explanation
DTDStatus 00	—	**Discrete Tone Detector Status** This location indicates the status of the tone detectors when in TONE DETECT mode (Configuration Register bits 6–0 (MODE) is 02H). Bit 0 indicates the status of detector 0, bit 1 (the status of detector 1), and so on. This location is only valid when in TONE DETECT mode. The response time of the tone detectors is dependent at the frequency of the tone being detected and sampling rate of the data pump. When the host sets Configuration Register bits 6–0 (MODE) is 0 (STANDBY), or resets the data pump, the data pump writes its part number into this location.

Transmitting Tones

The data pump features two tone generators, each with their own transmit level, as shown in Figure 9. The outputs are mixed together. The frequency of the tones are programmed by writing coefficients to locations ToneGenA and ToneGenB. The transmit levels are programmed by writing values to the DTMF Low Band Transmit Level (`DTMFl_lev`) and the DTMF High Band Transmit Level (`DTMFh_lev`). If only one tone is to be transmitted, the other tone generator's transmit level is set to 0 to disable it.

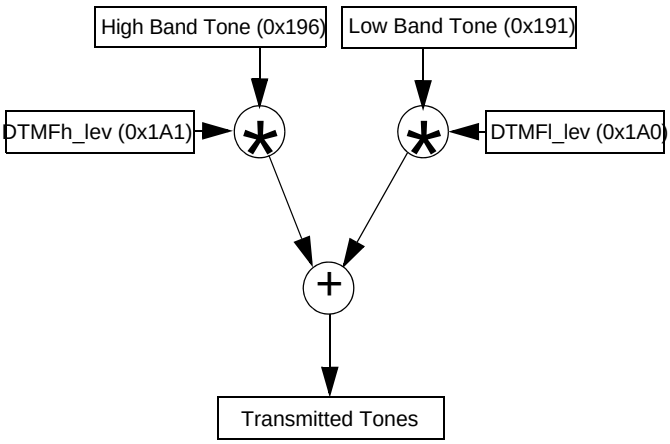


Figure 9. Transmitting Tones

For example, to generate a 2100 Hz Answer Tone for 3.3 seconds at –10dBm:

1. Set the ToneGenA Register to `015FEh`.
2. Set the DTMFl_lev Register to `0287h`.
3. Set the DTMFh_lev Register to `0`, disabling Tone Generator B.
4. Set Configuration Register bits 6–0 (MODE) to `1` (TRANSMIT TONE).
5. Wait 3.3 seconds, then set Configuration Register bits 6–0 (MODE) to 0 (STANDBY).

Tone Detectors

There are 16 tone detectors in the data pump. They are programmed by setting up one word for each tone detector. There is one global threshold setting for all 16 tone detectors. The addresses for the tone detectors are:

- Tone Detector Coefficients—`0145–0154h` (`Tone0–Tone15`)
- Tone Detector Receive Levels—`026h–035h` (`DTD0lev–DTD15lev`)
- Tone Detector Threshold–`03h`
- Tone Detector Status–`00h`

The tone coefficients are calculated as follows:

$$coeff_{tone} = \cos\left(\frac{2\pi \cdot f_{tone}}{9600}\right) \cdot 32767$$

The default values on reset are represented in Table 50.

Table 50. Tone Detector Default Values

Tone Detector	Frequency Detected (Hz)
0	697
1	770
2	852
3	941
4	1209
5	1336
6	1477

Table 50. Tone Detector Default Values (Continued)

Tone Detector	Frequency Detected (Hz)
7	1633
8	1750
9	1800
10	1650
11	2225
12	2250
13	1300
14	2100
15	600

The threshold is calculated as follows where level is in dBm:

$$\text{Threshold} = 10^{(\text{level})/20} \cdot 32767$$

The default value for the threshold is –24dBm. This value is set every time Configuration Register bits 6–0 (MODE) is set up to detect tones. If the user requires a different value, it must be reloaded after Configuration Register bits 6–0 (MODE) is set to detect tones.

To use the tone detectors, observe the following procedure:

1. Write the tone detector coefficients (DTD0 and DTD1 registers, 0145–0154H).
2. Set Configuration Register bits 6–0 (MODE) to tone detect mode (02H).
3. Set up the DTDThresh tone detector threshold.
4. Inspect the tone detector status.
5. When the detection phase is complete, set Configuration Register bits 6–0 (MODE) to standby (00H).

The detectors are set up as illustrated in Figure 10.

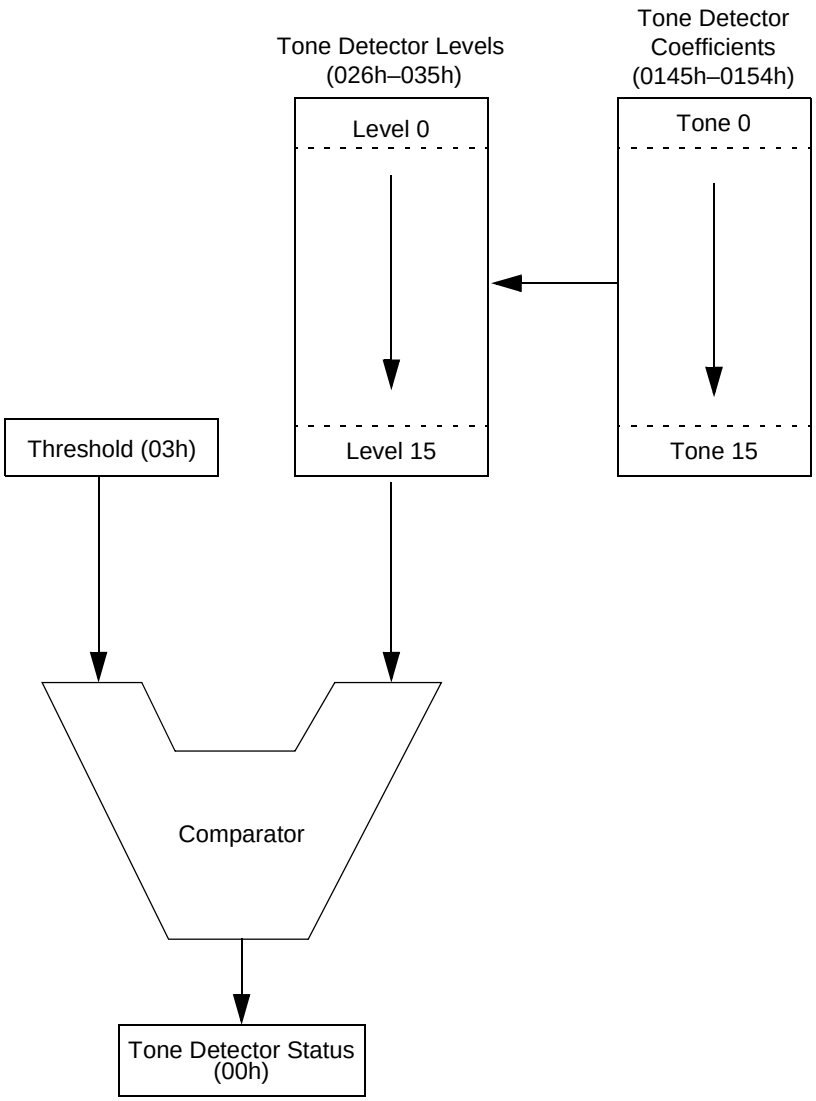


Figure 10. Tone Detectors

Note: Tone Detect mode is the same mode that is used for Biquad tone detectors because both detectors can run concurrently. As a result, the host is allowed to look for individual answer tones as well as call-progress tones.

Call-Progress Monitoring Using Biquad Tone Detectors

The data pump contains two biquad tone detectors that are capable of detecting energy in a frequency band. These detectors are useful for call-progress monitoring, where the exact frequency of the incoming signal is not known. Each biquad tone detector is composed of two cascaded, independently programmable, biquad sections. The order of biquad coefficients in RAM is:

b2, b1, a3, a2, a1, B2, B1, A3, A2, A1

The addresses for the coefficients for the two sections start at `0155h` (TONEA) and `015Fh` (TONEB). The sample rate is 9600 Hz.

The transfer equation for each section of the biquad tone detector is of the form:

$$H_n = \frac{2(a_1 + a_2 Z^{-1} + a_3 Z^{-2})}{(1 - 2b_1 Z^{-1} - 2b_2 Z^{-2})}$$

There are two threshold settings affecting both biquad tone detectors. The locations BiQuadOffThresh and BiQuadOnThresh define the on and off hysteresis points:

1. BiQuadOffThresh–052h–OFF point.
2. BiQuadOnThresh–051h–ON point.

Use the following formula to set the thresholds where level is in dBm:

$$\text{Threshold} = 10^{(\text{level})/20} \cdot 32767$$

The default values are –35 dBm (BiQuadOnThresh) and –42 dBm (BiQuadOffThresh).

The biquad tone detector status is contained in the ToneStatus Register bit 15 (TONEA) and ToneStatus Register bit 14 (TONEB). The response time of the biquad tone detectors depends on the coefficients and the input signal frequency.

The biquad tone detectors can be cascaded to form one tone detector with 4 biquad sections (an 8th order IIR filter) by setting ToneStatus Register bit 13 (CASCADE). In this case, ToneStatus Register bit 15 (TONEA) contains the status of the cascaded tone detector, and ToneStatus Register bit 5 (SQRDIS) controls whether the output of biquad tone detector B is squared before being input to biquad tone detector A.

The default settings for the biquad tone detector coefficients are indicated in Table 51 and Table 52, where the first row is TONEA and the second row is TONEB. The data pump sets the biquad tone detector coefficients to their default settings at any reset.

Table 51. Biquad Section 1 Coefficients (Hex)

Band (Hz)	b2	b1	a3	a2	a1
245–650	C774	7601	0716	F5FB	0716
360–440	C148	7A66	FF5C	0000	00A4

Table 52. Biquad Section 2 Coefficients (Hex)

Band (Hz)	B2	B1	A3	A2	A1
245–650	C63E	6FE1	F8EA	0000	0716
360–440	C7CD	7438:0	01AA	FEBC	01AA

To use the Biquad tone detectors to perform Call-Progress Monitoring, execute the following:

1. Set the coefficients. Coefficients that are changed remain valid until the next reset.
2. Set Configuration Register bits 6–0 (MODE) to 2 (detect tones). The biquad tone detectors and the discrete tone detectors operate simultaneously to allow the host to look for call-progress tones and individual answer tones at the same time.
3. Set the BiquadOnThresh and BiquadOffThresh values.
4. If the two biquad tone detectors are to be cascaded, set the ToneStatus Register bit 13 (CASCADE) to 1. If required, set ToneStatus Register bit 5 (SQRDIS) to 1 to disable the squarer when the tone detectors are cascaded.
5. Inspect ToneStatus Register bit 15 (TONEA) and ToneStatus Register bit 14 (TONEB) for the detection status. If ToneStatus Register bit 13 (CASCADE) is 1, only inspect ToneStatus Register bit 15 (TONEA.).
6. Time the ON time and the OFF time of the tone (s) to provide the cadence, which is used to identify the type of call-progress tone detected. For example, 0.5 second on, 0.5 second off is usually a BUSY tone.
7. After call-progress monitoring is complete, set Configuration Register bits 6–0 (MODE) to 0 (standby).

Dialing

The data pump may be programmed to dial using either DTMF tones, or make/break pulses. By default, the data pump is configured for tone (DTMF) dialing.

Tone Dialing

Tone dialing may be either continuous or timed. Continuous dialing generates the required tone until the host specifically shuts it off. Timed dialing allows the host to specify the on/off timing of the digit dialed.

The following example assumes the host controls the data pump's RTS through RAM Control and Status Register bit 3 (RTSP). To enable tone dialing, perform the following procedure:

1. Set RAM Control and Status Register bit 3 (RTSP) to 0, BiQuad Tone Sector Control Status Register bit 4 (TIMEDIAL) to 1 for timed dialing, or to 0 for continuous dialing. Then, set Configuration Register bits 6–0 (MODE) to 3 (dial). If timed dialing is required, set the timer locations Seq1Count and Seq2Count.
2. Control the twist by setting the DTMFh_lev and DTMFl_lev registers to specify the transmit levels of the High tone and the Low tone, respectively.
3. Set up the digit to be dialed in ToneStatus bits 3–0 (DIGIT) according to Table 53.

Table 53. Tone Dialing

Digit	Value
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
*	10
#	11
A	12
B	13
C	14
D	15

4. For continuous operation, set RAM Control and Status Register bit 3 (RTSP) to 1 to start transmitting the DTMF tone, and to 0 to stop.

5. For timed operation, set RAM Control and Status Register bit 3 (RTSP) to 1 to dial the digit. The data pump sets Modem Status Register bit 4 (DPBUSY) to 1 while it dials the digit. Set RAM Control and Status Register bit 3 (RTSP) to 0 after the digit has been dialed. The data pump sets Modem Status Register bit 4 (DPBUSY) to 0 when the dial sequence is completed.
6. To dial additional digits, repeat the procedure starting at Step 3.
7. When dialing is complete, set Configuration Register bits 6–0 (MODE) to 0 (standby).

The Z02922 data pump exhibits limited maximum output power. This feature applies not only to the data mode, but also to DTMF and other tone generation. During DTMF or tone generation, if the sum of the transmit levels programmed into DTMFh_lev and DTMFl_lev exceeds 30720 (0x7800) the data pump may not transmit the tones.

When transmitting DTMF with a required twist (the power difference between high and low bands), use this formula to determine the maximum DTMF transmit levels where x is the DTMF low band (DTMFl_lev) transmit level in dBm, and x+b is the DTMF high band (DTMFh_lev) transmit level in dBm (b is the twist in dBm):

```
10^(x/20) + 10^((x+b)/20) ¨ 30720/32768
```

The values for maximum transmit levels (DTMFl_lev + DTMFh_lev = 30720) at common twist values appear in the following table:

DTMFl_lev	DTMFh_lev	x	x+b	b
14,477	16,243	-7.10	-6.10	1
13,599	17,121	-7.64	-5.64	2
12,733	17,987	-8.21	-5.21	3

Pulse Dialing

Pulse dialing is similar to timed dialing, with this exception; the tone generated is a cadence of pulses output on the $\overline{OH}$ pin and mirrored in RAM location MStatus.OFF-HOOK. To implement pulse dialing, follow the instructions for timed tone dialing, except:

1. Select pulse instead of tone dial mode by setting the ToneStatus Register bit 4 (TONE-DIAL) to 0. Setting bit 4 to 1 has no effect. Pulse dialing is always timed.
2. After setting Configuration Register bits 6–0 (MODE) to 3 (dial), set Seq1Count, Seq2Count, and Seq3Count to the required make and break times, pausing after each digit is dialed. For North American applications requiring a 100msec cadence, a 39%/61% make/break ratio, and a 0.75 second pause, set locations Seq1Count to 024AH, Seq2Count to 0176h, and Seq3Count to 01C20h.

Manual Handshake Procedures

The V.22bis data pump software allows the host to control every aspect of the handshake procedure. The host instructs the data pump which signal to send at which time. The data pump sets status bits when it receives signals from the remote modem.

The host begins a manual handshake by setting Configuration Register bit 10 (MCUCTRL) to 1 to prevent the data pump from transmitting its own handshake signals.

The host monitors the receive signal status bits in location Trnctrl and transmits its own responding signals by setting Training Control Register bits 2–0 (TXCTRL) transmits the values described in Table 54.

Table 54. Signal Transmit Values

TRNCTRL Value	Signal Transmitted
0	Silence
1	1200 bps Unscrambled Binary 1
2	S1
3	1200 bps Scrambled Binary 1
4	2400 bps Scrambled Binary 1
5	1200 bps data mode or FSK
6	2400 bps data mode
7	2225 Hz tone

In Table 55, certain acronyms are used to denote the various V.22bis handshake signals.

Table 55. Handshake Acronyms

Name	Meaning
USB1	Unscrambled Binary 1
SB1	Scrambled Binary 1
S1	S1 Signal

Originating Modem

1. Take the telephone line off-hook and dial.
2. Program the discrete tone detectors and the biquad tone detectors for answer tones (2100 Hz) and call-progress tones (200–600 Hz). Look for both the answer tone and call-progress tones (such as busy tones, ring back and so on).

3. At receiving the 2100Hz answer tone, set Configuration Register bits 6–0 (MODE) to 4409H (V.22, V.22bis originate, manual handshake).
4. Wait for Training Control Register bit 5 (USB1DET) to become 1 (USB1 detected) continuously for 155msec.
5. Wait for 456msec.
6. Set Training Control Register bits 2–0 (TXCTRL) to 2 (transmit S1 signal) for 100msec.
7. Set Training Control Register bits 2–0 (TXCTRL) to 3 (transmit SB1), and inspect Trnctrl bit 6 (S1DET) and Trnctrl bit 7 (SB1DET) repeatedly for either a received S1 signal or SB1. If SB1 is received for 270msec, proceed to Step 11. If S1 is received, wait for the S1 to end. Proceed to wait for an additional 450msec.
8. Set Trnctrl bit 3 (V22BIS) to 1 (force a 16-way receive decision). Wait for 150msec.
9. Set Training Control Register bits 2–0 (TXCTRL) to 4 (transmit SB1 at 2400bps). Wait for 200msec.
10. Set Training Control Register bits 2–0 (TXCTRL) to 6 (2400bps data mode). Data is now transmitted and received at 2400bps.
11. In Step 7, if SB1 is detected instead of the S1 signal, wait for 765msec. Proceed to set Training Control Register bits 2–0 (TXCTRL)=5 (1200bps data mode). Data is now being transmitted and received at 1200bps.

Answering Modem

1. At a ring signal or a command from the host, take the phone off-hook and transmit silence for 1.8 to 2.5 seconds.
2. If required, use the tone generators to transmit a 2100Hz tone for 2.6 to 4 seconds. This tone is the V.25 answer tone.
3. Set Configuration Register bits 6–0 (MODE) to 0 (standby) and transmit silence for 75msec.
4. Set Configuration Register bits 6–0 (MODE) to 8 (answer mode, manual handshake). After setting Config, the host should be prepared to receive data from the remote modem. The data pump holds the received data to marks (that is, receives nothing) until the modem is able to receive data from the remote modem.
5. Set Training Control Register bits 2–0 (TXCTRL) to 1 (transmit USB1).
6. Inspect Trnctrl bit 6 (S1DET) and Trnctrl bit 7 (SB1DET) repeatedly for either a received S1 signal or SB1. If SB1 is received continuously for 270msec, proceed to Step 12. If an S1 signal is received (Trnctrl bit 7 (S1DET) to 1) wait for the S1 to end.

7. Set Training Control Register bits 2–0 (TXCTRL) to 2 (transmit S1 signal) for 100msec.
8. Set Training Control Register bits 2–0 (TXCTRL) to 3 (transmit SB1) for 350msec.
9. Set Trnctrl bit 3 (V22BIS) to 1 (force 16-way receive decisions), and wait for 150msec.
10. Set Training Control Register bits 2fl0 (TXCTRL) to 4 (transmit SB1 at 2400bps), and wait for 200msec.
11. Set Training Control Register bits 2–0 (TXCTRL) to 6 (2400bps data mode). Data is now being transmitted and received at 2400bps.
12. If in Step 6, SB1 is received instead of an S1 signal, set Training Control Register bits 2–0 (TXCTRL to 3 (transmit SB1) for 765msec. Then, set Training Control Register bits 2–0 (TXCTRL) to 5 (1200bps data mode). Data is now transmitted and received at 1200bps.

Making a V.22BIS Connection

In the following example, all timing is performed by the host.

Originating Modem

1. Take the telephone line off-hook and dial.
2. Program the discrete tone detectors and the biquad tone detectors for answer tones (2100Hz) and call-progress tones (200–600Hz). Look for the answer tone and call-progress tones (busy tones and ring back).
3. At receiving the 2100Hz answer tone, set Configuration Register bits 6–0 (MODE) to `4008h` (V.22bis originate). After setting Configuration Register bits 6–0 (`MODE`), the host should be prepared to receive data from the remote modem. The data pump holds the received data to marks (receives nothing) until the modem is able to receive data from the remote modem.
4. When the data pump establishes a V.22bis connection, and is ready to transmit data to the remote modem, it sets Reg5, Modem Status bit 1 (CDET) to `1`. Data may now be transmitted or received between the modems.

Answering Modem

1. At a ring signal or command from the terminal, take the phone off-hook and transmit silence for 1.8–2.5 seconds.

2. If required, use the tone generators to transmit a 2100 Hz tone for 2.6–4 seconds. This tone is the V.25 answer tone.
3. Set Configuration Register bits 6–0 (MODE)=0 (standby) and transmit silence for 75 msec.
4. Set Configuration Register bits 6–0 (MODE) to 8 (V.22bis answer). After setting Configuration Register bits 6–0 (MODE), the host is prepared to receive data from the remote modem. The data pump holds the received data to marks (receives nothing) until the modem is able to receive data from the remote modem.
5. When the data pump establishes a V.22bis connection, and is ready to transmit data to the remote modem, it sets Reg5, bit 1 (CDET) to 1. Data may now be transmitted or received between the modems.

Notes:
1. The data pump sets Reg5 bit 1 (CDET) to `0` during carrier dropouts, retrains, and when the remote modem hangs up the telephone line. Depending on the data mode, the host may use Reg5 bit 1 (CDET), Reg5 bit 2 (RTRND), Data Pump Miscellaneous Control Register bit 4 (EQE), EQMlev and EQMMaxThresh to determine when the remote modem has initiated a retrain, or has hung up the telephone line.
2. During 2400 bps V.22bis data mode, the host can use Dpctrl.EQE and EQMMaxThresh or EQMlev to determine when to initiate a retrain (see MStatus bit 11 RETRAIN) to improve the quality of the connection.

Using HDLC

The data pump includes HDLC firmware operating in all data modes. The HDLC firmware performs all the necessary operations to frame host-supplied data into HDLC format, including automatic opening and closing flag generation, zero insertion and deletion, flag and abort detection, and CRC checksum computation and checking.

HDLC Operation

During HDLC operation, the data pump frames host-supplied asynchronous data into a synchronous data stream in the transmitter, and extracts the same asynchronous data from the received synchronous data stream in the receiver. The inclusion of 16-bit cyclic redundancy check (CRC) information in the frames allows the receiving host to check whether the data has been correctly received.

HDLC data is sent in frames. A frame consists of a number of bytes, each composed of 8 data bits. A frame contains an opening flag, frame data bytes, two CRC checksum bytes,

and a closing flag, respectively. Opening flags and closing flags indicate the start and the end of a frame, respectively.

A flag, byte value 07EH, is one of two HDLC control symbols. The other is an abort, which is any sequence of consecutive binary 1s more than six bits long. If the frames do not use the bandwidth of the data mode (for example, when there is no host data to transmit), the modem fills the remaining bandwidth by sending flags between frames.

Frame data bytes for transmission are supplied by the host to the data pump's DATAP Register. These bytes are modified by the data pump to ensure that no more than five consecutive binary 1 bits are sent. To accomplish this modification, the transmitting modem inserts a single 0 bit after every five consecutive binary 1 bits in the host supplied data. This zero insertion process allows the receiving modem's data pump to distinguish between frame data, flags, and aborts. The receiving modem's data pump uses a zero deletion process to remove each inserted 0 bit before returning the data to the receiving modem's host.

When a frame is to be closed, the frame's two CRC checksum bytes are sent immediately following the frame data. The CRC checksum is computed without the inserted 0s. The frame's closing flag is transmitted following the CRC. This flag may also serve as the opening flag of the next frame, which saves bandwidth.

Enabling HDLC Operation

The data pump's HDLC firmware is disabled at power-up and any reset, and can be enabled only in parallel mode (Reg4 bit 4 TPDM to 1). To enable HDLC, set Bufctrl bit 7 HDLC to 1, and bits 8–15 of Bufctrl to 0 prior to beginning data mode operation. The host reads Register DATAP before starting data mode to clear DATAP.

These examples demonstrate the use of the data pump in parallel mode to transmit and receive HDLC data frames. The examples assume that the data pump has just been put in data mode and HDLC operation is enabled. The data to be sent or received is the sequence of N bytes {Byte1–ByteN}, where Byte1 is sent (or received) first.

Transmitting

1. When Reg5 bit 5 (TXI) is 1, write Byte1 to DATAP. Repeat this Step for each byte to be transmitted. If Reg4 bit 7 (TXIE) is 1, the data pump generates an interrupt when it is ready to transmit the next byte, for example, when the byte sets Reg5 bit 5 (TXI) to 1.
2. When the last byte, ByteN, has been sent, wait for the data pump to set Reg7 bit 2 (TEND) to 1. This function indicates that the data pump has closed the current frame. The data pump now computes and transmits the CRC checksum and closing flag for the frame. The data pump does not set Reg7 bit 2 (TEND) to 1 until at least 8 bit-times after it has set Reg4 bit 6 (TXI) to 1, indicating the data pump is ready to transmit another data byte. To transmit another frame, repeat steps 1–2.

3. When the data pump begins sending the frame's closing flag, it sets Reg7 bit 2 (TEND) to 0. Transmission of the frame is complete 8 bit-times after the data pump sets Reg7 bit 2 (TEND) to 0.

Receiving

1. Prepare to receive a new frame.
2. When Reg5 bit 6 (RXI) is 1, the data pump has received a byte. First Read Register Reg7, followed by DATAP. Register 7 is read first, because the data pump may change it at any time after DATAP is read. If Reg4 bit 6 (RXIE) is 1, the data pump generates an interrupt when it sets Reg5 bit 6 (RXI) to 1.
3. Act on the value of the Reg7 read in Step 2, as follows:
   a. If bit 1 (RXERROR) is 0 and bit 0 (EOF) is 0, then the DATAP value read in Step 2 is an HDLC frame byte. Repeat Step 2 to receive all remaining frame bytes.
   b. If bit 1 (RXERROR) is 0 and bit 0 (EOF) is 1, then an HDLC frame with a correct checksum has been received. If Byte1–ByteN+3 were read, with ByteN+3 being the DATAP value just read, then the two previous bytes (ByteN+1 and ByteN+2), are the frame checksum bytes; the remaining bytes (Byte1–ByteN) are the frame data bytes. Continue from Step 1 to receive the next frame. If bit 1 (RXERROR) is 1, discard any received frame bytes and continue from Step 1 to receive the next frame.
   c. If DATAP was 0FF, an HDLC abort sequence was received. If DATAP was `07EH`, an HDLC frame with an incorrect checksum was received.

Data Pump Firmware Version Number and Part Number

The data pump code version can be obtained any time the RAM Location Configuration Register bits 6–0 (MODE) is set to 0. The data pump writes the part number to data pump RAM location 0 and the code version number to the DATAP Register. To obtain the version and part number from the data pump, the following steps must be performed:

1. Set Configuration Register bits 6–0 (MODE) to 0 (STANDBY), then read location Config to provide the data pump enough time to begin standby operation.
2. Read the DATAP Register. This register returns the code release version number (an 8-bit value, for example, `030h` indicates version 30).
3. Read RAM location 0. This location returns the part number (for example, `02922h` for a Z02922 part).

Sleep Mode

The data pump incorporates a low-power SLEEP Mode. In this mode, the data pump clock is shut down, effectively stopping the part. To enter SLEEP Mode, the controller can set Configuration Register bits 6–0 (MODE) to mode 7. To exit SLEEP Mode, the controller can either reset the data pump (asserting the RESET signal) or write any value to the DATAP Register. The host should then wait at least 2 msec before accessing the data pump registers.

V.29 Quick Connect Handshake

The data pump provides a V.29 Quick Connect Mode. This mode is a half-duplex synchronous 9600 bps modulation scheme, allowing the host to change the direction of the data flow quickly. When used with a suitable host data transfer protocol, it can provide a fast pseudo full duplex channel.

The data pump characterizes the telephone line connection by performing a long training sequence before the first exchange of data in each direction. Subsequent training sequences are quicker because they make use of characteristics determined during the previous long training sequence.

V.29 Quick Connect is a half-duplex mode. Only one modem transmits a carrier at any given time. Whenever training is performed, both modems must be set to perform the same type of train, either long or short.

This example assumes that a telephone connection has been established, the host is using parallel mode, and the host controls the data pump's RTS through RAM Control and Status Register bit 3 (RTSP). The description of Register RAM Control and Status Register bit 3 (RTSP) explains the host's options for controlling the data pump's RTS signal.

To Transmit

1. Before transmitting for the first time in each direction (in each modem) after a telephone connection has been established, set Dpctrl bit 13 (TXSTRN) to 0 for a long train. For subsequent short retrains, set Dpctrl bit 13 (TXSTRN) to 1. Then set Configuration Register bits 6–0 (MODE) to `020h` (9600 bps V.29) or `021h` (7200 bps V.29). Then set RAM Control and Status Register bit 3 (RTSP) to 1 to cause the data pump to begin transmission.
2. Set Configuration Register bit 12 (ECHOPRTEN) and Configuration Register bit 12 (ECHOPRTLEN) at the same time as Configuration Register bits 6–0 (MODE), to transmit an echo protect tone if required.

3. Inspect Reg5 bit 1 (CDET). When Reg5 bit 1 (CDET) is 1, the host may begin transmitting data. If parallel mode transmit interrupts are required, set Reg5 bit 7 (TXIE) to 1.
4. When required, set RAM Control and Status Register bit 3 (RTSP) to `0` to end transmission. Wait for Modem Status Register bit 4 (DPBUSY) to become `0` to indicate the data pump has completed transmission before beginning receiving or hanging up the telephone line.

To Receive

1. Before receiving for the first time in each direction (in each modem) after a telephone connection has been established, set Dpctrl bit 12 (RXSTRN) to 0. Then set Configuration Register bits 6–0 (MODE) to `020h` (9600bps V.29) or `021h` (7200bps V.29). Set RAM Control and Status Register bit 3 (RTSP) to 0 to cause the data pump to begin reception.
2. Inspect Reg5 bit 1 (CDET). When Reg5 bit 1 (CDET) is 1, the host may begin receiving data. If parallel mode transmit interrupts are required, set Reg5 bit 6 (TXIE) to 1.
3. Receive data for at least 50msec, then set Dpctrl bit 12 (RXSTRN) to 1 to cause the data pump to receive a shortened subsequent retrain sequences. Do not set Dpctrl bit 12 (RXSTRN) to 0 between trains or another long train must be executed even if Dpctrl bit 12 (RXSTRN) is restored to 1 before the next train.
4. When the data pump loses carrier, it sets Reg5 bit 1 (CDET) to 0. Wait for Reg5 bit 1 (CDET) continuously for at least 50msec before assuming reception has ended. After reception has ended, the host may switch the data pump to begin transmitting, or hang up the telephone line.

V.29 Handshake

The data pump also provides a standard ITU V.29 mode. This mode is a half-duplex synchronous 9600bps/7200bps modulation scheme, allowing the host to change the direction of the data flow quickly. When used with a suitable host data transfer protocol, it can provide a fast pseudo-full-duplex channel.

This example assumes that a telephone connection has been established, the host is using parallel mode, and the host controls the data pump's RTS through RAM Control and Status Register bit 3 (RTSP). The description of Register RAM Control and Status Register bit 3 (RTSP) explains the host's options for controlling the data pump's RTS signal.

To Transmit

1. After a telephone connection has been established, set Dpctrl bit 12 (TXSTRN) to 0. Then set Configuration Register bits 6–0 (MODE) to 020h (9600bps V.29) or 021h (7200bps V.29). Then set RAM Control and Status Register bit 3 (RTSP) to 1 to cause the data pump to begin transmission.
2. Set Configuration Register bit 12 (ECHOPRTEN) and Configuration Register bit 12 (ECHOPRTEN) at the same time as Configuration Register bits 6–0 (MODE), to transmit an echo protect tone if required.
3. Inspect Reg5 bit 1 (CDET). When Reg5 bit 1 (CDET) is 1, the host may begin transmitting data. If parallel mode transmit interrupts are required, set Reg5 bit 7 (TXIE) to 1.
4. When required, set RAM Control and Status Register bit 3 (RTSP) to 0 to end transmission. Wait for Modem Status Register bit 4 (DPBUSY) to 0 to indicate the data pump has completed transmission before beginning receiving or hanging up the telephone line.

To Receive

1. After a telephone connection has been established, set Dpctrl bit 12 (RXSTRN) to 0. Proceed to set Configuration Register bits 6–0 (MODE) to 020H (9600bps V.29) or 021H (7200bps V.29). Set RAM Control and Status Register bit 3 (RTSP) to 1 to cause the data pump to begin reception.
2. Inspect Reg5 bit 1 (CDET). When Reg5 bit 1 (CDET) is 1, the host may begin receiving data. If parallel mode transmit interrupts are required, set Reg5 bit 7 (TXIE) to 1.
3. When the data pump loses carrier, it sets Reg5 bit 1 (CDET) to 0. Wait for Reg5 bit 1 (CDET) continuously for at least 50msec before assuming reception has ended. After reception has ended, the host may switch the data pump to begin transmitting, or hang up the telephone line.

Typical Performance Data

The Bit Error Rate (BER) and Block Error Rate (BLER) curves in Figure 11 and Figure 12 represent typical performance over a variety of signal to noise conditions (SNR).

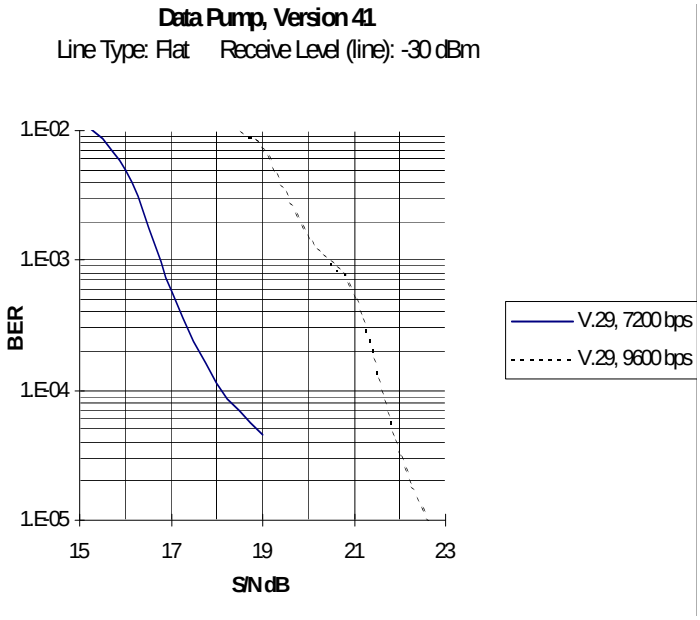


Figure 11. V.29 Typical Performance Data

Note: Modems usually exhibit lower bit-error rates receiving in the low band as opposed to the high band.

When an analog link is made, the Adaptive Equalizer (AEQ) is frozen. The noise level is then increased without making new links. These tests were conducted using a Consultronics TCS500 Telephone Line Simulator, and a Hewlett Packard 4951B protocol analyzer/ BERT tester under the conditions described in Table 56.

Table 56. Performance Testing Conditions

Line Simulation	Flat
Transmit Level	–10 dBm
Receive Level	–16.0 dBm
Data Transmitted	511 Pseudo-Random Pattern
Number of Bits Sent	1,000,000
Number of Blocks Sent	1,000
Bits per Block	1,000
AEQ	Frozen after Link Establishes
Noise Calibration	C-Message

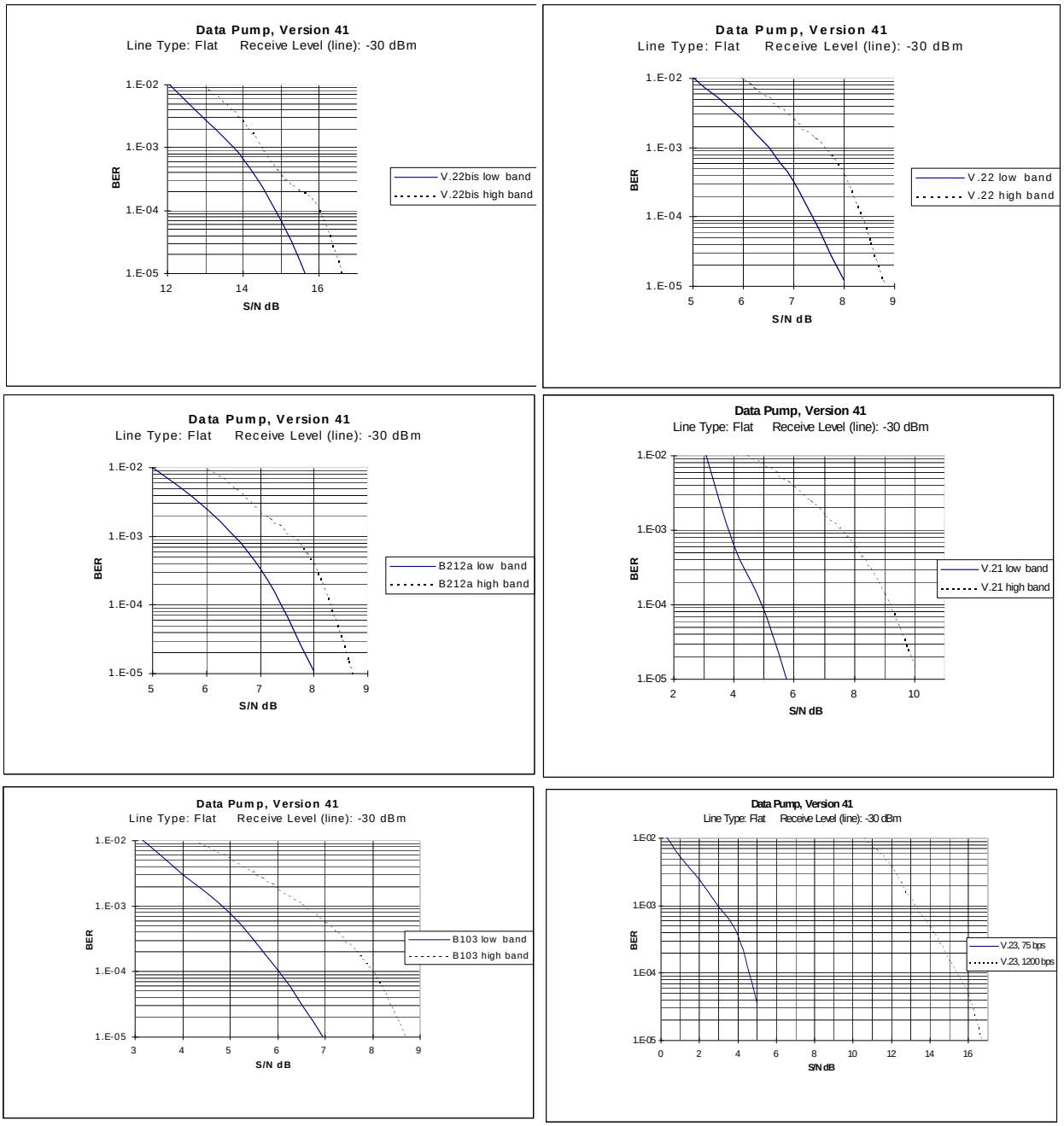


Figure 12. Typical Performance Data

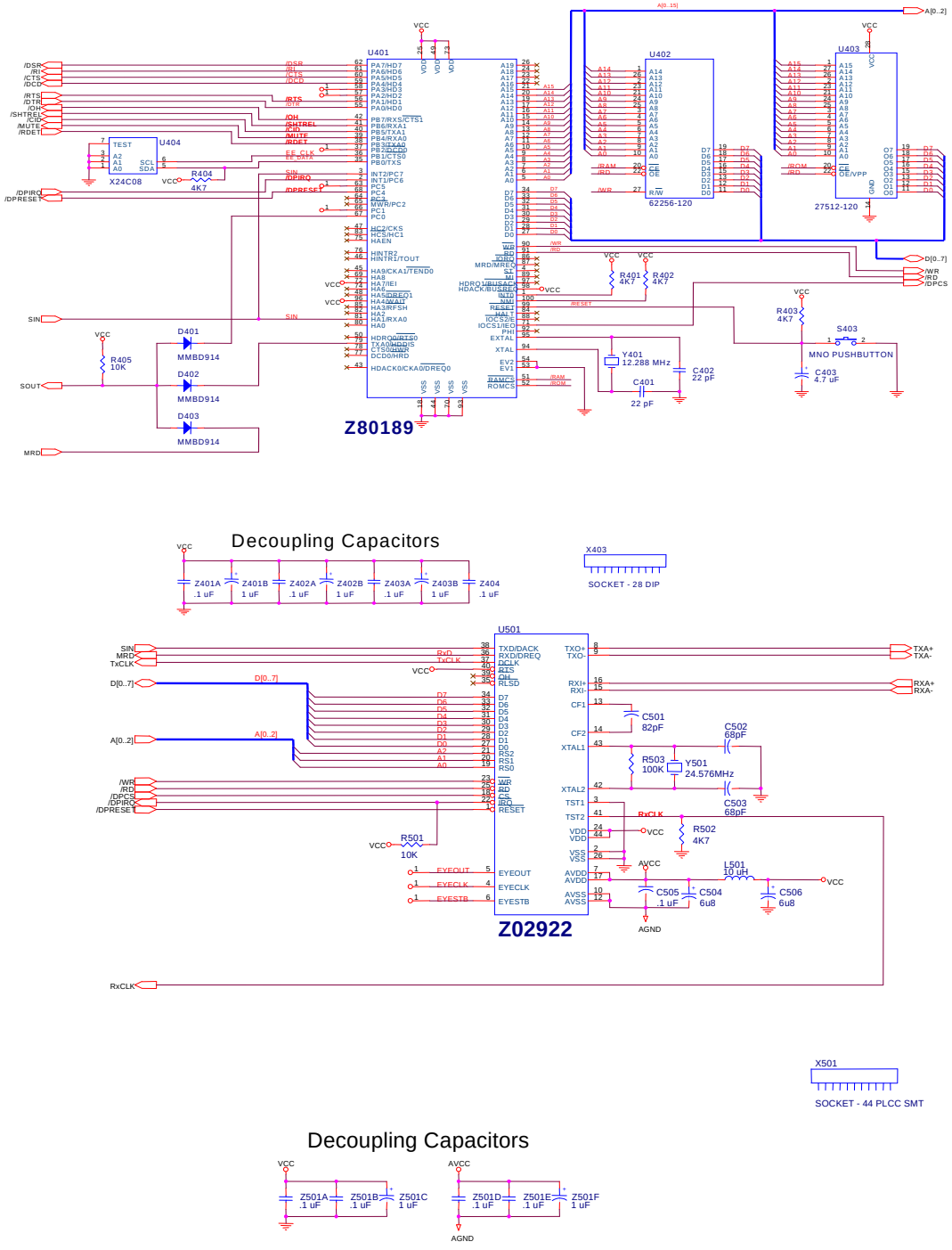


Figure 13. Example Modem Using Z02922 and a Z189 Microcontroller

Example DAA

Figure 14 is an example DAA configuration for North America. Isolation transformer, T1, couples the primary (line) and secondary (modem) sides, while providing high- voltage isolation. This wet transformer (allowing DC current) simplifies the circuit, while reducing the cost of the DAA.

On the Secondary side, the transmit (TxA+ and TxA–) and receive (RxA+ and RxA–), are combined in the 4-wire to 2-wire hybrid circuit. This hybrid can be either passive or active. The more complex active hybrid allows operation to lower signal levels. It cancels out most of the transmit signal from the receive signal.

On the Primary side, the off-hook relay switches the phone line between a local handset (PHONE) or the modem. The ring detect circuit consists of DC blocking capacitor C4, current limiting resistor R2, zener diodes CR3 and CR4, optocoupler U3, and its reverse protection diode D3. Protection elements RV1, F1, C1, and C2 (and transformer T1's isolation) provide higher voltage capability for approval in some foreign markets. C1 and C2, for example, may must be replaced by Metal Oxide Varistors (MOV's) or Gas Discharge Tubes (GDTs). The shunt relay reduces the DAA impedance during pulse dialing. This operation is required for certain country approvals.

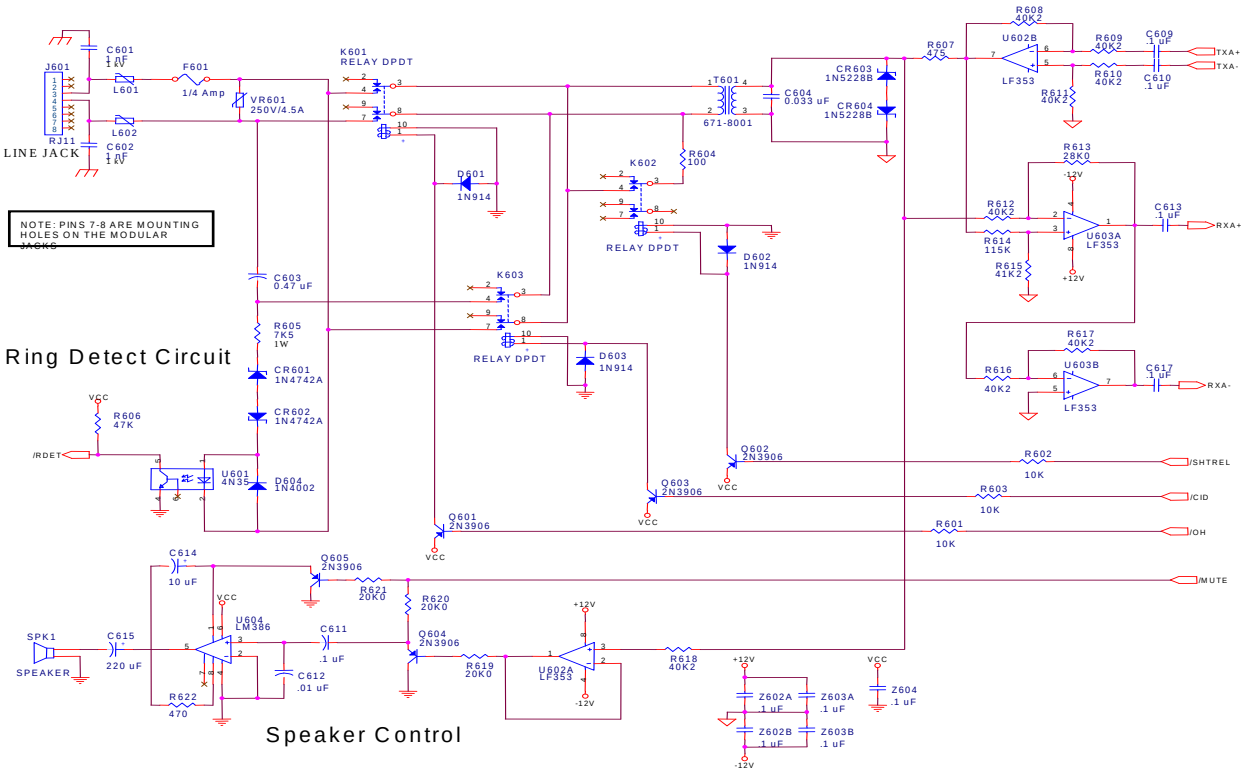


Figure 14. Example DAA

Eye Pattern Circuit

Figure 15 shows a typical eye pattern circuit for the Z02922. The Z02922 Eye Pattern port consists of 3 signals:

- Data (EYEOUT):The most significant and least significant bytes of this 16-bit word are the X and Y coordinates respectively for the eye pattern display. Each byte is most significant bit first.
- Clock (EYECLK): Data is set on the rising edge of the EYECLK, and should be read on the falling edge.
- Strobe (EYESTB): This signal is active Low when the data is valid.

Data is shifted through a pair of 8-bit serial-in parallel-out shift registers (74HC594) in response to the falling edge of EYECLK, then latched into a pair of 8-bit DACs on the rising edge of EYESTB. The output of these DACs can be viewed on an oscilloscope in X–Y mode to see the received signal quality.

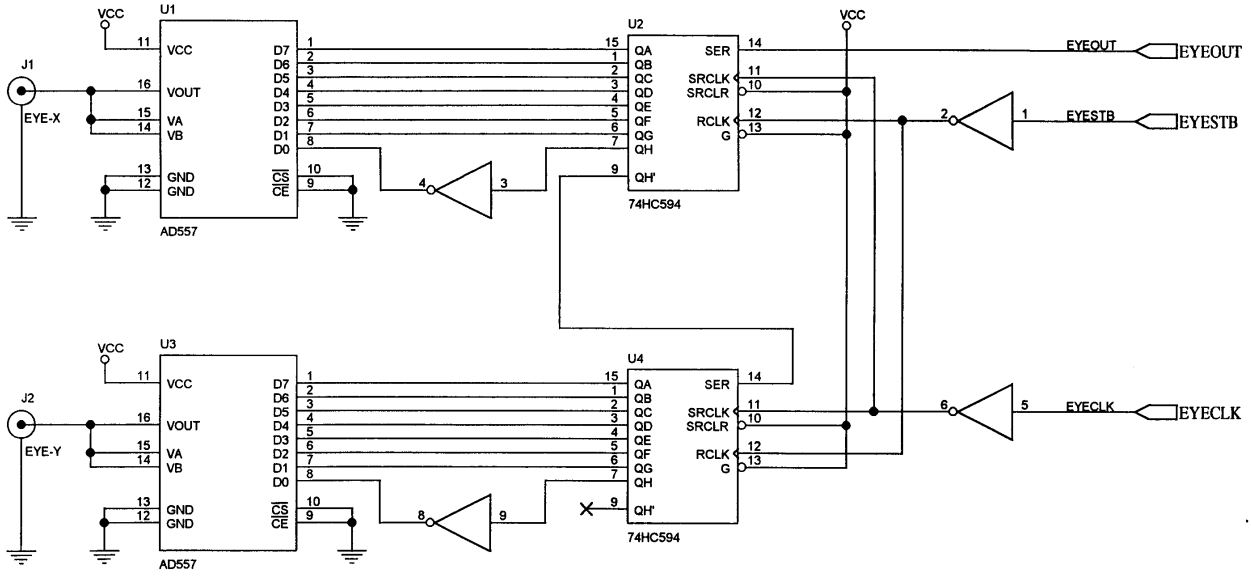
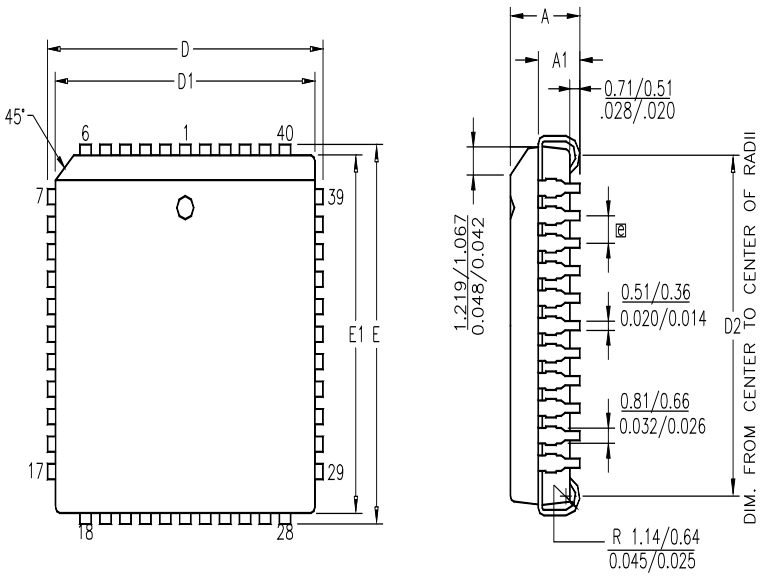


Figure 15. Eye Pattern Circuit

Package Information



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 16. 44-Lead PLCC Package Diagram

Ordering Information

The 12.288 MHz Z02922 device in the 44-Pin PLCC package is available in two ROM Code versions:

ROM Code Version	ROM Code Reference
0x42	Z0292212VSCR3910
0X3A	Z0292212VSCR3796

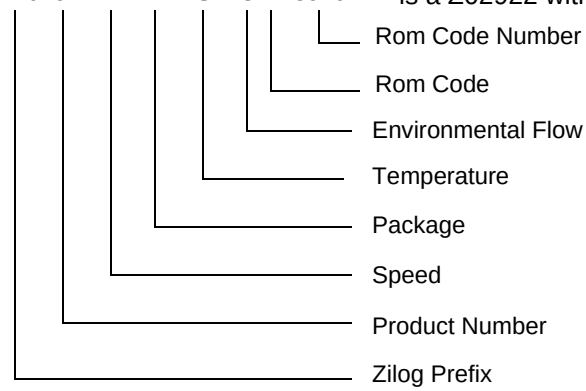
For fast results, contact your local Zilog sales office for assistance in ordering the part you require.

Codes

Speed	12 = 12.288 MHz
Package	V = Plastic Leaded Chip Carrier
Temperature	S = 0°C to +70°C
Environmental	C = Plastic Standard
ROM Code	R3910 = ROM code number 3910 (ROM code Version 0x42) R3796 = ROM code number 3796 (ROM code Version 0x3A)

Example

Z 02922 12 V S C R 3910 is a Z02922 with ROM code R3910, 12.288 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow



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